A PROTOTYPE OF A NEW CLASS OF OVERSAMPLING ADC

A Thesis

by

JUN HE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2005

Major Subject: Electrical Engineering

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Approved as to style and content by:

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Yoonsuck Choe (Member)	Chanan Singh (Head of Department)

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ABSTRACT

A Prototype of a New Class
of Oversampling ADC. (May 2005)
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Chair of Advisory Committee: Dr. Takis Zourntos

Analog-to-digital (A/D) and digital-to-analog (D/A) converters are important blocks in signal processing system because they provide the link between the analog world and digital systems. Compared with Nyquist-rate data converters, oversampling data converters are more desirable for modern submicron technologies with low voltage supplies. Today, all existing oversampling modulators in popular use are derived from sigma-delta modulation. Stability is the most significant problem in the sigma-delta modulator, because the ultimate accuracy is limited by stability. As the aggressiveness of the design increases, the margin of stability diminishes rapidly.

This thesis presents the design and experimental results of the first prototype circuit implementation of the novel oversampling modulation scheme proposed by Dr. Takis Zourntos. This new class of oversampling modulators are theoretically stable. With less stability limitation, the new class of modulators can potentially achieve higher signal-to-noise ratio (SNR) or less power by designing the modulator more aggressively. This thesis describes the methods and procedures of how the new oversampling modulation theory is implemented into a circuit. Some novel circuit architectures are proposed in this modulator, such as a filter which can provide status outputs for the controller and realize arbitrary zeros and poles, comparators with synchronization latches to eliminate the effect of metastability, and a digital-to-analog

converter (DAC) with current calibration circuits for high linearity.

A third-order continuous-time oversampling modulator employing 4-bit quantization is implemented in a 0.35-μm double-poly complementary metal oxide semiconductor (CMOS) technology, with a chip area of 2150×2150 μm^2. Simulation results show it achieves 83.7-dB peak SQNR, 90-dB dynamic range over a 500kHz input signal bandwidth, and 60 mW power consumption.

To the people who love me

ACKNOWLEDGMENTS

With gratitude, I acknowledge many people who contributed their time, effort, and expertise to help me in this work.

First I would like to express my sincere gratitude to my advisor, Dr. Takis Zourntos, for the great opportunity to work under his guidance, and for his enthusiasm and inspiration. This work would not have been possible without the support and encouragement from him.

I wish to thank Dr. Jose Silva-Martinez and Dr. Edgar Sanchez-Sinencio. They brought me into this exciting field of analog and mixed circuit design.

I would like to thank Dr. Aydin Karsilayan. He helped me a lot in Candence setup and circuit design.

I'm grateful to Dr. Ugur Cilingiroglu and Sualp Aras for their generous help in my chip taping out.

I would like to thank Dr. Sameer Sonkusale for his valuable discussions in comparator design.

Very special thanks to Ella Gallagher for her kind assistance in many aspects.

My work benefited greatly from my fellow students, who provided me with generous support: Xiaofeng Wang, Nebu John Mathai, Shanfeng Chen, Jinghua Li, Jianhong Xiao, Tianwei Li, Timothy Fischer, Johnny Lee, Burak Kelleci, Xuemei Liu, Xiaohua Fan, Artur Lewinski, Ari Y. Valero-Lopez, Alberto Valdes-Garcia, Wenchang Huang and Jianglong Chen. Xiaofeng spent much time discussing technical issues and providing many good suggestions for my design. Nebu helped me with most of the digital circuits design in this project. Shanfeng, Jinghua and Burak helped me with circuit design and tool issues. Jianhong is my nearest officemate. I learned much about many areas of analog circuit design from him. Tianwei helped me in testing

the chip. Tim was always patient in helping me with Cadence issues.

I would like to thank the following friends for their friendship and support: Haitao Tong, Lin Chen, Bing Zhao, Boran Zhao, Tong Zhu, Jiong Wu, Guang Zhang. They made my experience at Texas A&M University enjoyable and fruitful.

I would like to acknowledge the professors and staff in the Department of Electrical Engineering who helped me with academics and my life here.

I also wish to thank the other members of my degree committee, Dr. Narasimha Reddy and Dr. Yoonsuck Choe for providing me with excellent feedback and their time spent on the committee.

Finally, I would like to thank my parents and my family for their love and constant encouragement.

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CHAPTER I

INTRODUCTION

A. Background and Motivation

Digital signal processing has proliferated because of its flexibility, reproducibility, reliability and programmability. With the rapid evolution in modern semiconductor technology, digital signal processing systems have a lower overall cost compared to analog systems [1] [2]. In many areas analog circuits are replaced by their digital counterparts such as wireless communication and digital audio. But as the interface between the real physical world and virtual digital world, A/D and D/A converters are always required.

Data converters can be divided into two main types: Nyquist-rate converters and oversampling converters. Recently, oversampling converters have become popular with the booming low-power low-voltage CMOS mixed-signal system-on-chip (SoC). They accomplish analog-to-digital or digital-to-analog conversion but are mainly digital circuits. They do not require high-precision analog circuitry as traditional Nyquist-rate converters do. Thus they are more desirable for modern submicron technologies with low voltage supplies.

Now almost all existed oversampling modulators in popular use are derive from the sigma-delta modulation. The oversampling sigma-delta modulator, first proposed by Cutler in 1954 [3], is based on two important concepts, oversampling and noise-shaping, both of which are understood in the frequency domain.

Some problems exist in practical sigma-delta modulators such as idle tones and stability. Idle tones result when the quantization noise contains discrete spectral

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lines. Stability is one of the most significant problems in the sigma-delta modulators, because the ultimate accuracy is limited by stability. As the aggressiveness of the design increases, the margin of stability diminishes rapidly [4] [5].

To address the stability problem in sigma-delta modulation, Dr. Takis Zourntos proposed a new approach to oversampling encoding based on nonlinear control theory [6] [7]. This proposed architecture is inspired by formulating the problem of data conversion as a tracking-control problem. A stabilizing controller is adopted to minimize quantization error and that provides overall converter stability. We will refer to this new oversampling modulator as the Nonlinear Control-based Oversampling modulator (NCO modulator).

B. Significance of This Work

This work is significant because this is the first circuit implementation of the NCO modulator. This oversampling encoding is cost-effectively achieved without the use of sigma-delta modulation and represents a step towards a more stable oversampling converter. The NCO modulator can potentially achieve higher signal-to-noise quantization ratio (SQNR) by allowing a more aggressive shaping of quantization noise. In circuit design, it also means we can use less power for the given specifications (SQNR, signal bandwidth) by decreasing oversampling ratio (OSR) thus decreasing the sampling clock frequency.

Also we can expect this novel scheme can be widely used in digital-to-analog conversion, Class-D power amplifiers, phase-locked loop (PLL) and other signal processing devices in which sigma-delta modulators are used. This work can provide some valuable insights for future work.

C. Aims of the Research

This thesis introduces the circuit implementation of the NCO modulator. The main target of this research is to develop a prototype circuit to make the theory practical. Specifically we:

1. develop and optimize the prototype third-order 4-bit oversampling modulator for low-pass analog-to-digital conversion in system-level, which is suitable for IC development;
2. find a practical way to realize all the blocks in system-level into circuits; and
3. propose a hardware prototype of the NCO modulator in 0.35-μm CMOS technology.

D. Organization of the Thesis

The remaining chapters are organized as follows:

Chapter II introduces the fundamentals of oversampling modulation. Chapter III gives a plain explanation of the theory of the novel oversampling modulation proposed by Dr. Takis Zourntos [6] [7]. Chapter IV describes design of the prototype third-order 4-bit oversampling modulator for low-pass analog-to-digital conversion in system-level. Chapter V extends circuit design and experimental verification of the prototype oversampling modulator. Chapter VI introduces the layout design and provides the post-layout simulation results. Chapter VII summarizes this research and gives recommendations for future work.

CHAPTER II

FUNDAMENTALS OF OVERSAMPLING ANALOG-TO-DIGITAL CONVERSION

Data conversion provides the interface between the real, physical world and the virtual, digital world. A/D conversion is the process of sampling in discrete time and quantizing in magnitude on an analog input signal. A/D converters often appear as the bottleneck in mixed signal system.

According to the relationship between sampling frequency and signal bandwidth, A/D converters can be classified into Nyquist-rate and Oversampling A/D converters. This chapter introduces the fundamentals of Nyquist-rate and Oversampling A/D converters. Furthermore, we discuss the advantages and stability problem of sigma-delta A/D converters.

A. Introduction of Nyquist-Rate A/D Converters

Nyquist-rate A/D converters generate a series of output values in which each value has a one-to-one correspondence with an analog input signal. The Nyquist-rate defines the lowest sampling rate that will permit accurate reconstruction of a sampled analog signal. The sampling frequency of Nyquist-rate A/D converters is at, or slightly higher, than the Nyquist-rate.

The functional level diagram of Nyquist-rate A/D converters is shown in Figure 1.

An anti-aliasing filter is a filter that attenuates unwanted high-frequency signals (which otherwise would appear as undesired, aliased frequency components) of an analog signal prior to its conversion into a digital value. For Nyquist-rate A/D converters, anti-aliasing filters with steep brick wall type roll-off at the transition band are required because of the narrow transition band.

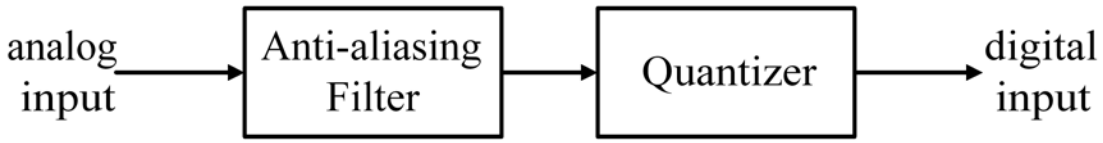

Fig. 1. Functional level diagram of Nyquist-rate A/D converters

For a quantizer shown in Figure 2, the equation that relates these signals [5] is

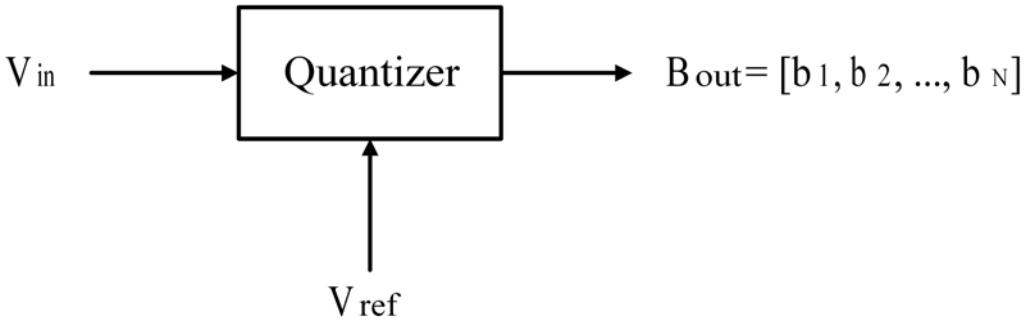

Fig. 2. A block diagram representing a quantizer

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = V_{in} \pm e, \tag{2.1}$$

where $-\frac{1}{2}V_{LSB} \leq e \leq \frac{1}{2}V_{LSB}, V_{LSB} \equiv \frac{V_{ref}}{2^N}$, e is quantization error.

Assuming the quantization error, e, is white noise, the probability density function, $f_e(x)$, for such an error is shown in Figure 3. We can analyze the power of e

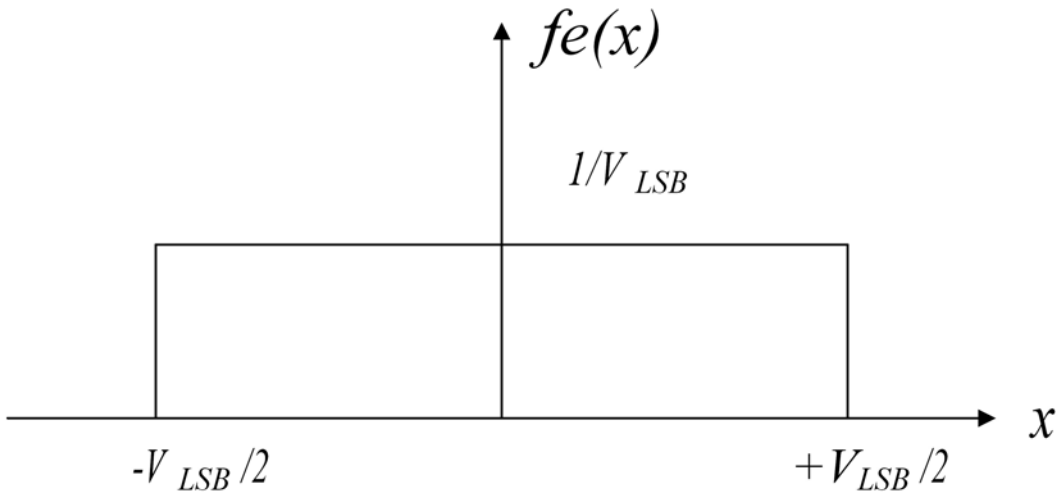

Fig. 3. Probability density function for the quantization error

as

$$e^2 = \int_{-\infty}^{+\infty} x^2 f_e(x) dx = \frac{1}{V_{LSB}} \left(\int_{-V_{LSB}}^{+V_{LSB}} x^2 dx \right) = \frac{V_{LSB}^2}{12}. \tag{2.2}$$

Assuming the input signal V_{in} is a sinusoidal waveform between 0 and V_{ref},

$$SQNR = 10log_{10} \left(\frac{V_{ref}^2/8}{V_{LSB}^2/8} \right) = 6.02N + 1.76, \tag{2.3}$$

where N is the number of quantizer bits.

Nyquist-rate converters are often difficult to implement in modern submicron technologies because they need precise analog components, and their circuits can be vulnerable to noise and interference.

B. Introduction of Oversampling A/D Converters

The sampling frequency of oversampling A/D converters is much higher than Nyquist-rate (typically 20 to 512 times [5]). The functional level diagram of oversampling A/D converters is shown in Figure 4.

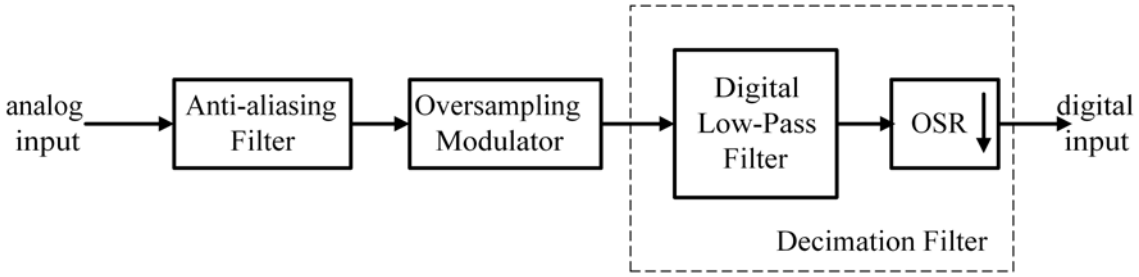

Fig. 4. Functional level diagrams of oversampling A/D converters

We use the following concepts in our discussion of oversampling A/D converters.

- OSR (oversampling ratio): $OSR \equiv f_s/2f_b$

  where f_s is the sampling rate, f_b is the input signal bandwidth.

- SQNR (signal to quantization noise ratio):

  $SQNR \equiv 10log$ (signal power/quantization noise power)

- SNDR (Signal to noise and distortion ratio):

  $SNDR \equiv 10log$(signal power/(quantization noise power+harmonic power))

- DR (dynamic range): The range, in dB, between the noise floor of a device and its defined maximum output level.

Compared with Nyquist-rate A/D converters, oversampling A/D converters can achieve high resolution with relatively coarse analog components. The realization of high-resolution analog circuitry is complicated by low power-supply voltages and poor transistor output impedance (caused by short-channel effects) for modern submicron technologies [5]. State-of-the-art low-cost semiconductor fabrication technologies usually provide 10-bit matching accuracy. However, oversampling converters can achieve better than 20-bit resolution with such technologies at the expense of lower frequency bandwidth and more complicated digital circuitry.

A second advantage of oversampling converters is that they simplify the requirement placed on the analog anti-aliasing filters. We can see it very clearly in Figure 5. Another advantage of oversampling converters is that the sample-and-hold stage is usually not required. Furthermore, the programmability of oversampling converters is better than that of Nyquist-rate converters. Oversampling converters can be configured conveniently for wider bandwidth with less resolution or narrower bandwidth with higher resolution.

C. Introduction of Sigma-Delta Modulation

Now almost all existed oversampling modulators in popular use are derive from the sigma-delta modulation. The block diagram of a sigma-delta modulator is shown in Figure 6 [6].

The basic concept of sigma-delta modulation is the use of feedback for improving the effective resolution of a coarse quantizer [5]. The effect of sigma-delta modulation can be estimated through the use of a pseudo-linear model, shown in Figure 7.

In this model a nonlinear operation, quantization, is replaced by the addition of a noise signal. In many practical situations, the linear model is accurate. But when

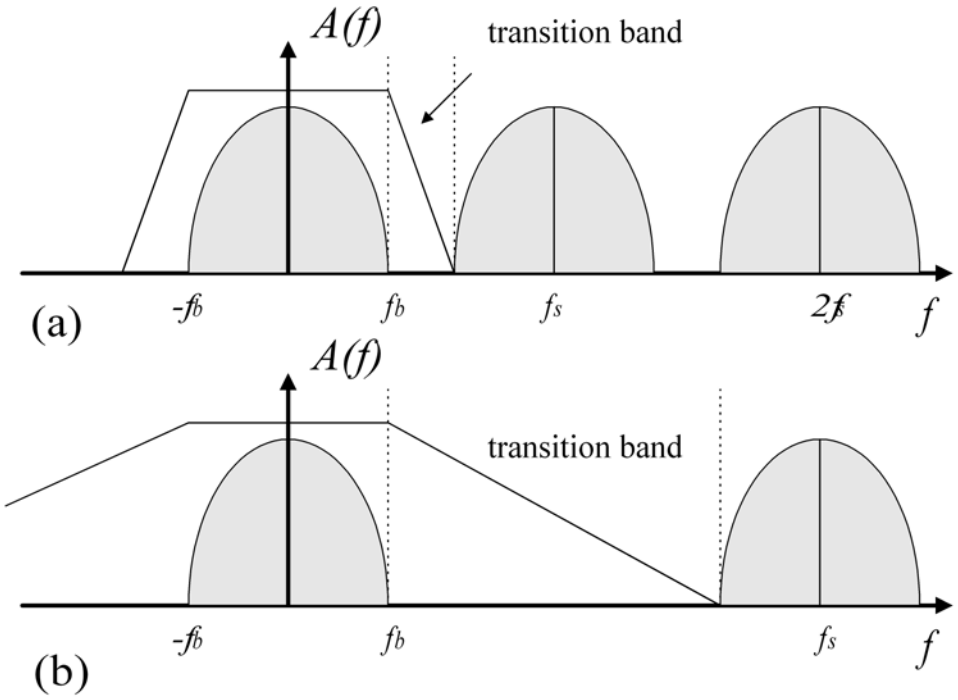

Fig. 5. Anti-alias filter requirements for (a) Nyquist-rate and (b) oversampling [8]

the noise no longer meets the white noise assumption, the linear model breaks down. Failures of the linear model cause problems such as idle-channel tones and instability in the modulator [4].

The most two important concepts in sigma-delta modulation are oversampling and noise-shaping.

1. Oversampling

Let's begin by modelling a quantizer. When the input $x(n)$ is very active, the quantization error, $e(n)$, can be approximated as an independent random number uniformly

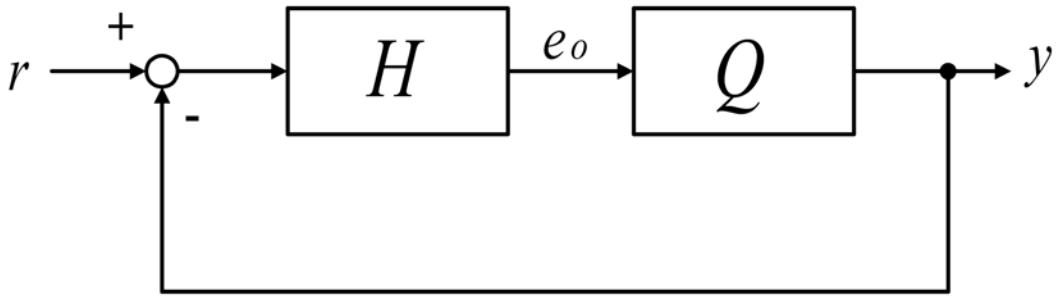

Fig. 6. Diagram of sigma-delta modulator

distributed between $\pm V_{LSB}/2$, where V_{LSB} equals the difference between two adjacent quantization levels. Thus the quantization noise power is given by $V_{LSB}^2/12$. The spectral density of $e(n)$ is shown in Figure 8.

Assuming the input signal bandwidth is f_0, and the sampling rate is f_s, we define the oversampling ratio, OSR, as $OSR \equiv f_s/2f_0$. The quantization noise power in the signal band is

$$Pe = \int_{-f_s/2}^{+f_s/2} S_e^2(f)df = \frac{V_{LSB}^2}{12 \times OSR} \tag{2.4}$$

Therefore, doubling OSR decreases the quantization noise power by one-half or, equivalently, 3dB.

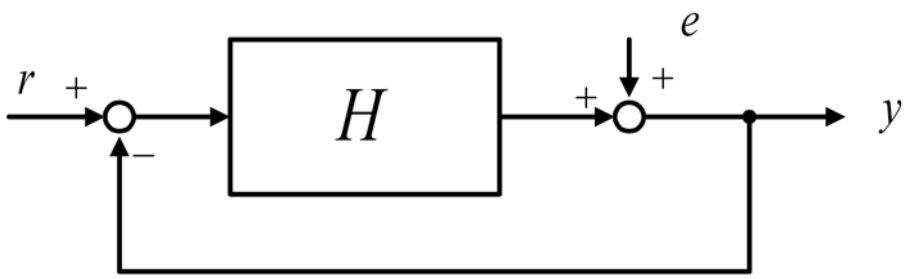

Fig. 7. Pseudo-linear model of sigma-delta modulator

2. Noise-Shaping

The pseudo-linear model of a general noise-shaping sigma-delta modulator is shown in Figure 7. The noise transfer function (NTF) is :

$$NTF = \frac{1}{1+H}. \tag{2.5}$$

To shape the quantization noise, we choose H such that its magnitude is large from 0 to f_0. With such a choice, the NTF will be approximately zero over the signal band. The high frequency noise is not reduced by the feedback as there is a little loop gain at high frequencies. However, additional post filtering can remove the out of band quantization noise with little effect on the desired signal.

As an example, let's consider a first-order noise shaping in which [5]

$$H(z) = \frac{1}{z-1}. \tag{2.6}$$

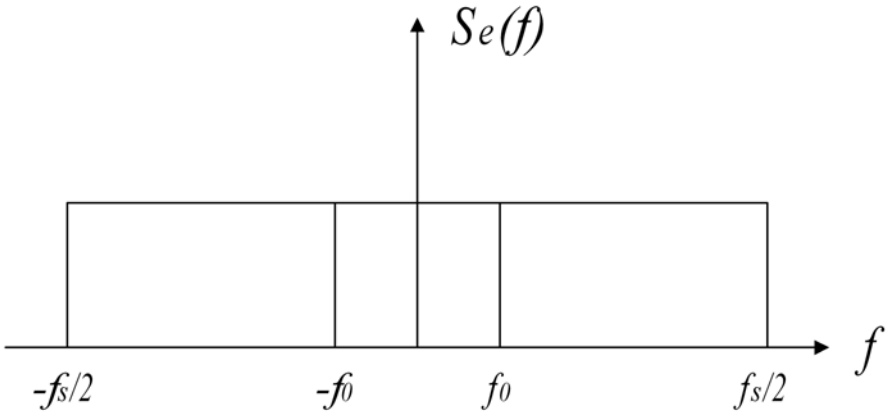

Fig. 8. Spectral density of $e(n)$

So

$$NTF(z) = \frac{1}{1 + 1/(z-1)} = 1 - z^{-1}. \tag{2.7}$$

Let $z = e^{j\omega T} = e^{j2\pi f/f_s}$, and we have

$$NTF(f) = sin\left(\frac{\pi f}{f_s}\right) \times 2je^{-j\omega f/f_s} \tag{2.8}$$

and

$$Pe = \int_{-f_s/2}^{+f_s/2} Se^2(f)|NTF(f)|df \approx \frac{\pi^2 V_{LSB}^2}{36}\left(\frac{1}{OSR}\right)^3. \tag{2.9}$$

Assume the input signal is a sinusoidal wave. For full-scale input, the signal power is

$$Pe = \left(\frac{2^N V_{LSB}}{2\sqrt{2}}\right)^2 = \frac{2^{2N} V_{LSB}^2}{8}. \tag{2.10}$$

Then the maximum SNQR is given by

$$SQNR_{max} = 10log\left(\frac{Ps}{Pe}\right) = 6.02N + 1.76 - 5.17 + 30log(OSR). \tag{2.11}$$

Therefore, doubling OSR decreases the quantization noise power by one-eight or, equivalently, 9dB. The maximum SQNR can be further increased as a function of OSR by using higher order filtering [4] [5]. This is an important property of sigma-delta modulators.

3. Stability Problem of Sigma-Delta Modulators

A stable modulator is defined as one in which the input to the quantizer remains bounded such that the quantizer does not become overloaded and the filter states are bounded.

The linear model of the sigma-delta modulator shown in Figure 7 is based on the assumption that quantization error, e, is white noise. When the assumption fails, the linear model breaks down. Failures of the linear model cause problems such as idle-channel tones and instability in the modulator. Tones result when the quantization noise contains discrete spectral lines. Stability is the most significant problem in sigma-delta modulators because it limits the ultimate accuracy. As the aggressiveness of the design increases, the margin of stability diminishes rapidly.

In sigma-delta modulation, the objective is to design the NTF to push the noise power from the signal band to high frequencies. The more aggressively the NTF is designed, the higher the achievable resolution. But the modulator may become unstable when the NTF increases. So there is a trade-off between the aggressiveness of the NTF and modulator stability. As a general rule of thumb, keeping NTF less than 1.5 often leads to a stable modulator with a 1-bit internal quantizer [5]. For this reason, the practical sigma-delta modulator can not achieve the maximum dynamic range predicted by theory.

4. Discrete-Time and Continuous-Time Sigma-Delta Modulators

The discrete-time sigma-delta modulators utilizing switched-capacitor circuit techniques are the majority of sigma-delta modulators. It is an attractive solution because the design of a switched-capacitor modulator is more straight forward and the loop parameters are tightly controlled due to the excellent matching of on-chip capacitors [4] [9].

There are also some disadvantages of switched-capacitor modulators. There are settling time constraints so that the switched-capacitor modulators can not achieve high operation speed. It requires high accuracy sampling network. The clock feedthrough and sampling distortion can not be attenuate by feedback. And the power consumption is high [10].

In contrast to a switched-capacitor modulator, a continuous-time modulator can potentially achieve higher sample rate or less power consumption because no settling behavior is involved. The accuracy requirement of sampling network is relaxed. In addition, the continuous-time modulator is intrinsic anti-alias filtering [11].

CHAPTER III

THEORY OF THE PROPOSED NOVEL OVERSAMPLING MODULATION SCHEME

This chapter summarizes content appearing in the papers by Dr. Takis Zourntos [6] [7]. It provides a simplified explanation of the theory to help the reader gain insight into the operation of the NCO modulator [12] [13] [14].

A. Introduction

As we discussed in the last chapter, one of the most significant problems in sigma-delta modulators is stability. The achievable signal-to-noise quantization ratio (SQNR) of sigma-delta modulator is often substantially lower than the known theoretical value because of stability constraints. The block diagram of a sigma-delta modulator is shown in Figure 6.

The principle of sigma-delta modulators is best understood in the frequency domain. Oversampling and noise-shaping are used to attenuate the noise power in the signal band. We do this by designing the signal transfer function (STF) and the noise transfer function (NTF) as shown in Figure 9 [6]. The STF is defined as $H/(1+H)$. The NTF is defined as $1/(1+H)$.

From a time domain point of view, the accuracy of the modulator is proportional to the difference between the input, r, and the output, y. The quantization error is equal to $y-r$. So our purpose is to minimize the average quantization error. This inspired Dr. Zourntos to consider it as a control problem. An appropriate controller can be designed to minimize the quantization error. In other words, the understanding of the modulator is transferred from the view point of a coding problem to the view point of a tracking-control problem.

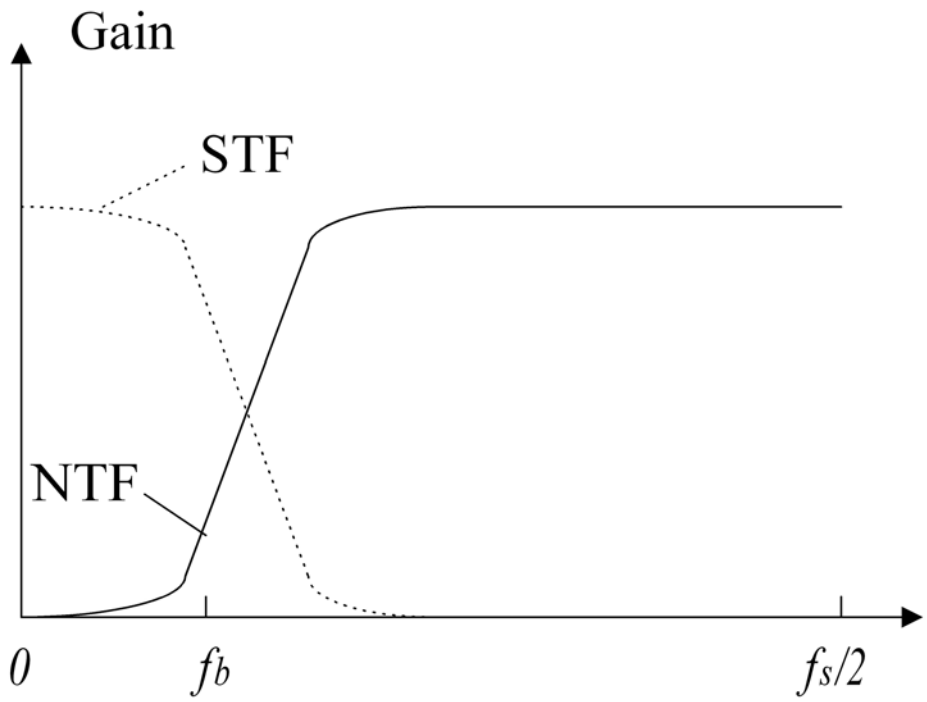

Fig. 9. STF and NTF for sigma-delta modulator

Based on the architecture of the sigma-delta modulator shown in Figure 6, a controller is inserted, which is used to minimize the conversion error, $e_o = H(r - y)$ in magnitude and provide overall system stability. If the size of e_o is made sufficiently small, the digital output signal y represents the signal r to within any desired accuracy.

The new system architecture is shown in Figure 10.

Based on nonlinear control theory Dr. Zourntos found a novel oversampling architecture which can achieve high resolution and improve system stability. The overall architecture is shown in Figure 11.

A controller C is inserted between the output of the filter H and the quantizer

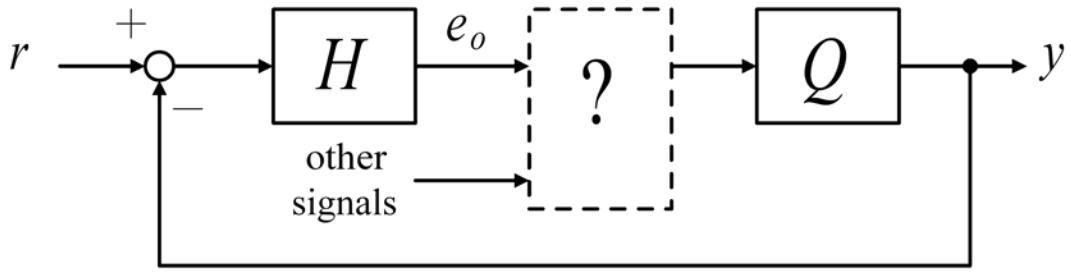

Fig. 10. Oversampling modulator with controller

Q.

B. Controller Design

Let's begin with some definitions and assumptions. We can express a filter in state space model as:

$$Filter: \begin{cases} \dot{x} = Ax + bu \\ y = cx \end{cases} \tag{3.1}$$

where x denotes the state vector of the filter, y denotes the output of the filter, u is input. A, b and c are the state-model matrices of the filter. In Figure 11 the filter H can be expressed as:

$$H: \begin{cases} \dot{e} = Ae + br \\ e_o = ce \end{cases} \tag{3.2}$$

where e denotes the state vector of H, e_o denotes the output of H, r is input. A, b and c are the state-model matrices of H.

The design of the controller is based on the methods of variable-structure theory,

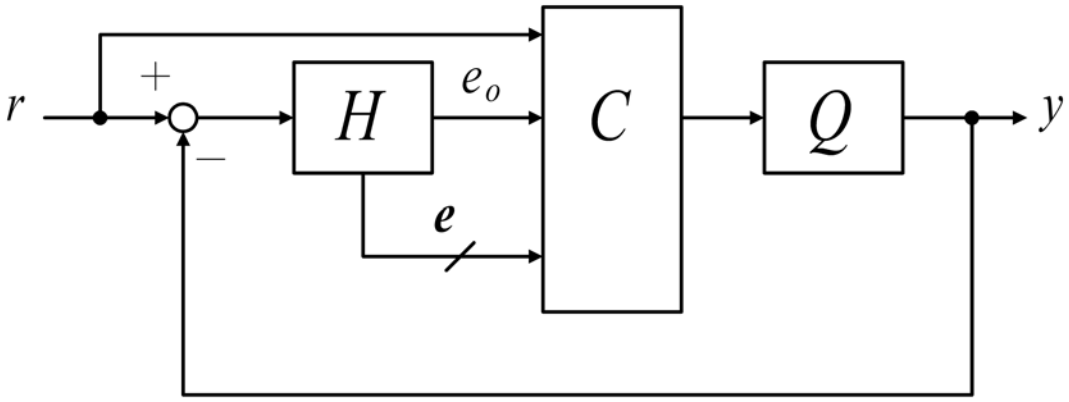

Fig. 11. Proposed oversampling modulator

in which a switching (nonlinear) control law is selected to ensure that the time-derivative of a Lyapunov-like function is negative.

Let's start with the noise power

$$V = \frac{1}{2}e_o^2 \tag{3.3}$$

where both sides are function of time t.

We want to design a controller such that we establish the condition $\dot{V} < 0$. Therefore the conversion error e_o would be minimized in magnitude.

Differentiate both sides of Eq. (3.3) with respect to time to obtain

$$\dot{V} = e_o\dot{e}_o. \tag{3.4}$$

Substituting Eq. (3.2) into Eq. (3.4) results in

$$\dot{V} = e_o c(Ae + b(r - y)) = e_o cAe + e_o cbr - e_o cby. \tag{3.5}$$

We write

$$y = y_c + y_q \tag{3.6}$$

in which y_c denotes our controller output and y_q the (bounded) quantization error. Then we can get

$$\dot{V} = e_o cAe + e_o cbr - e_o cby_c - e_o cby_q. \tag{3.7}$$

If we set

$$y_c = r + \frac{1}{cb}(k\text{sgn}(e_o) + cAe) \tag{3.8}$$

and substitute into Eq. (3.7), it yields

$$\dot{V} = -e_o cby_q - ke_o\text{sgn}(e_o) = -e_o cby_q - k|e_o|. \tag{3.9}$$

Here y_q can be positive or negative. But if we set k, where $k > 0$, large enough, this helps to ensure $\dot{V} < 0$. Notice $|y_q| < Mq$, where M_q $(0 < M_q < \infty)$ is a bound on the magnitude of the quantization error. Then we can obtain from Eq. (3.9)

$$\dot{V} < |e_o||cb|M_q - k|e_o| = -|e_o|(k - |cb|M_q). \tag{3.10}$$

We set $k = |cb|M_q + \varepsilon_k$ where ε_k is a non-zero positive constant. Then

$$\dot{V} < -|e_o|\varepsilon_k < 0. \tag{3.11}$$

From the above deduction, we get the design of controller shown in Figure 12.

It can be proved that the proposed oversampling modulator is stable and the magnitude of conversion error, e_o, is made small under such assumptions (the reader can refer to [6]):

1. The sampling rate of the system is infinite;

2. The initial condition, $e(0)$, satisfies $e(0) \in \mathbf{R}^n$;

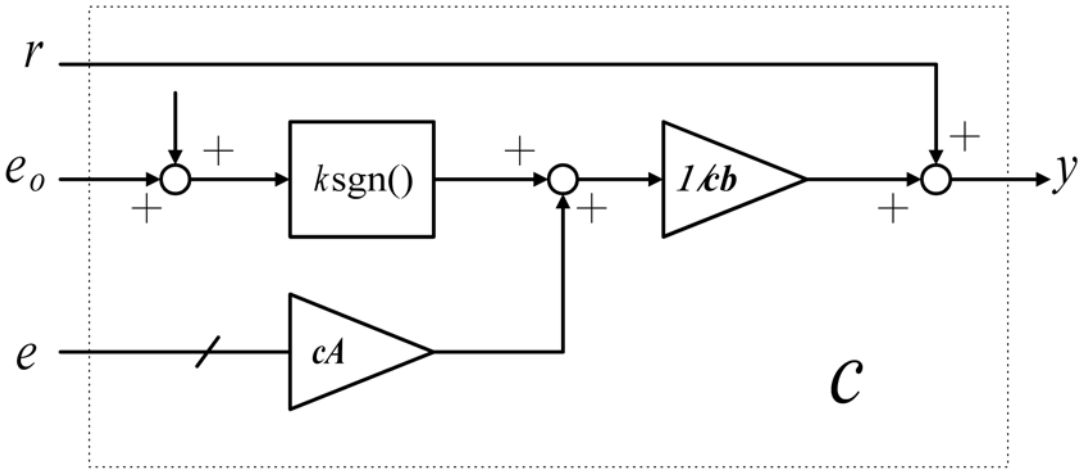

Fig. 12. Proposed nonlinear controller

3. The matrices A and c constitute a controllable pair;

4. The product cb is non-zero;

5. All zeros of H are in the open left-half plane;

6. The states of H are accessible;

7. The quantizer element, Q, does not saturate, and the magnitude of the quantization error is less than $M_q \in \mathbf{R}$ $0 < M_q < 1$;

8. The disturbance v is less than $\delta \in \mathbf{R}$, $\delta > 0$ in magnitude for all $t \geq 0$.

CHAPTER IV

DESIGN OF THE PROTOTYPE NCO MODULATOR AT THE SYSTEM LEVEL

In this chapter we introduce the design of the prototype third-order 4-bit NCO modulator for low-pass analog-to-digital conversion at the system-level.

A. Design Methodology

Figure 13 shows the block diagram of the NCO modulator.

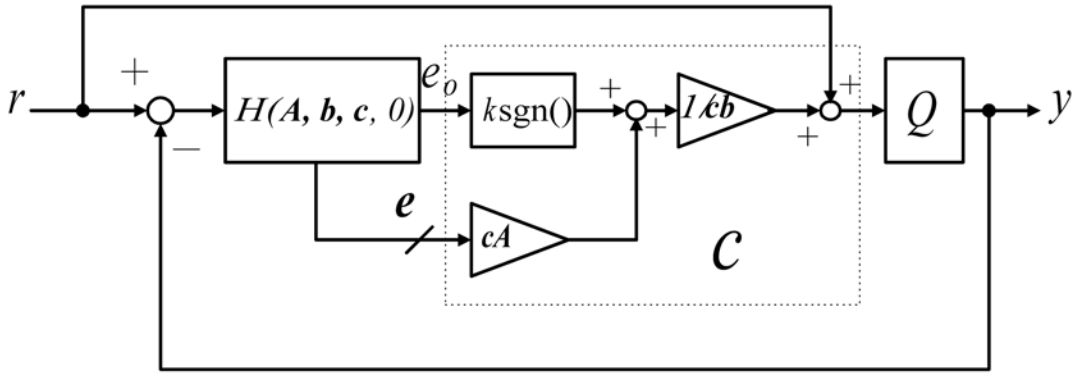

Fig. 13. Block diagram of the NCO modulator system

1. Introduction of System Parameters and Their Effects on the System

Before introducing the system-level modulator design, we will introduce the system parameters which is defined in the MATLAB scripts provided by Dr. Zourntos. We use these scripts to do system-level design.

f_s: Sampling rate (Hz). Signal band frequency $f_b = f_s/(2 * OSR)$.

OSR**:** Oversampling ratio. Increasing OSR yields improved SNR.

N**:** Order of H. Increasing order yields improved SNR.

R_s**:** Minimum stop-band attenuation of H (Elliptical Filter). Critical for performance. Increasing R_s yields improved SNR. However there's a limitation on R_s. The system becomes unstable if R_s is too high.

R_p**:** Passband ripple of H.

$shift$**:** This is the amount that we shift the zeros away from jw-axis. The value of shift should be between 1/10 to 1/100 of fs. Based on the simulation results we suggest select shift as follows [6]:

$$H = \begin{cases} \text{shift=0.015625fs} & \text{for 3rd order 1-bit} \\ \text{0.25fs} & \text{for 3rd order 3,5-bit} \\ \text{0.075fs} & \text{for 5th order} \end{cases} \tag{4.1}$$

sat_lim**:** Quantizer saturation limit.

$nlevels$**:** Number of levels in quantizer. Increasing nlevels yields improved SNR.

qi**:** Quantization interval size. $qi = (2 * sat\_lim)/nlevels$

k**:** Gain of sgn() block. It should be around $cb * qi$.

2. How to Optimize the Parameters for Highest Peak SQNR

Dr. Zourntos proposed the system-level design methodology of the NCO modulator in [6] [7]. The procedure to optimize the system for highest peak SQNR is summarized as follows:

1. Specify $f_s, OSR, N, nlevels$ (The default value: $sat\_lim = 1$, $k = cb * qi$, Rp=2 or 3);

2. Set Rs as a low value such as 30dB; set shift according to Eq (4.1);

3. Simulate the system and obtain the SQNR while increasing the magnitude of input sinusoid signal from -20dB to 0dB . Obtain the peak SQNR.

4. Increase Rs. Then do Step 3 again. If the new peak SNR is higher than last one, continue return to Step 3. If the new peak SNR is lower than last one, then we choose the last value of Rs. Go to Step 5.

5. Adjust shift around the original value. Return to Step 3 and find the highest peak SNR.

B. Characteristics of the NCO Modulator

Figure 14 shows the typical time domain behavior of the NCO modulator. The top plot is the input sinusoidal signal. The middle plot is the conversion error e_o. The bottom plot is the quantizer output, which is also the modulator output.

We do a FFT on the modulator output data and get the spectrum plots shown in Figure 15. The top plot shows the spectrum up to one-half of sampling rate. The bottom plot shows spectrum in signal-band.

After optimizing the system we get the relationship between SQNR and OSR. Figure 16 and Figure 17 show the results for the third-order and fifth-order modulators. We see that the peak SQNR ramps up linearly with the (logarithm) of OSR, around 20dB/octave for the 3rd-order modulator and 30dB/octave for the 5th-order modulator.

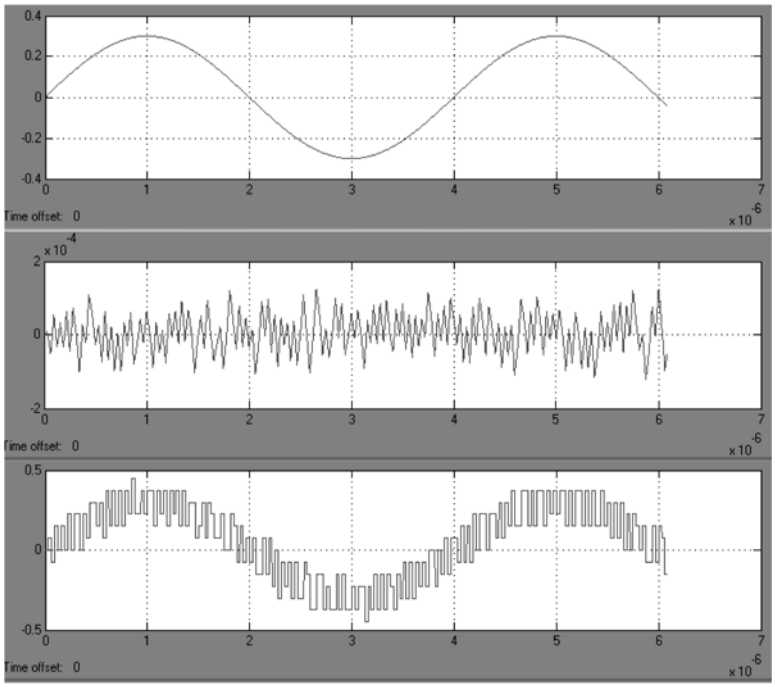

Fig. 14. Typical time domain behavior of the NCO modulator

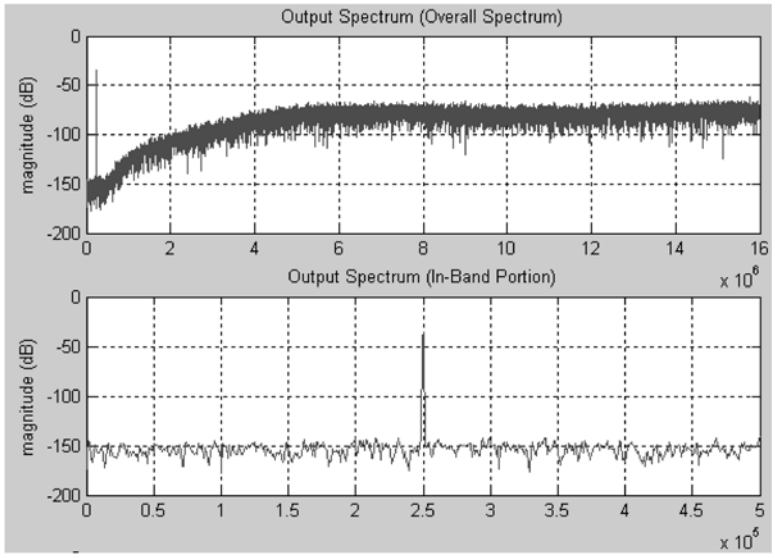

Fig. 15. Output spectrum of the NCO modulator

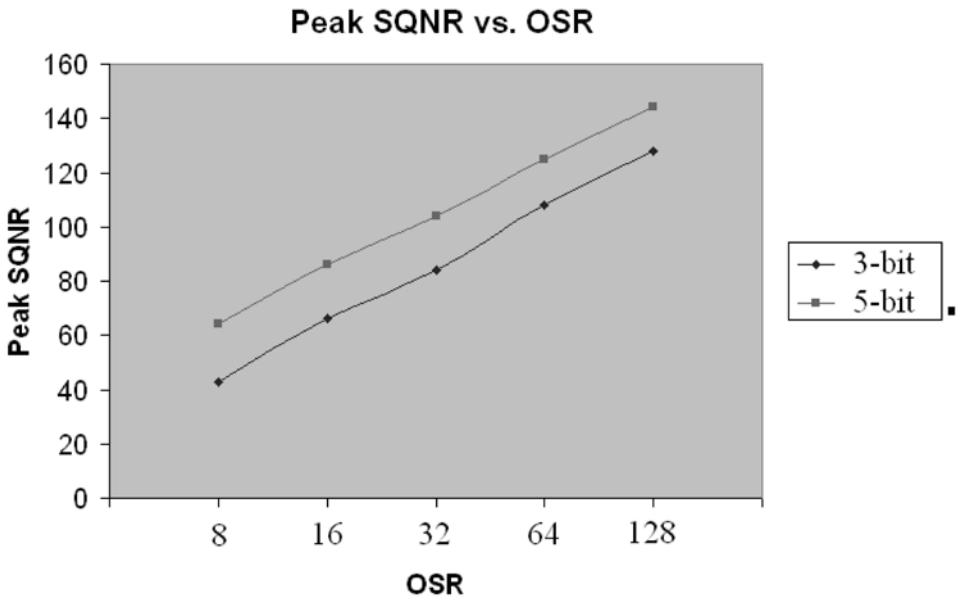

Fig. 16. Peak SQNR vs. OSR for third-order modulator

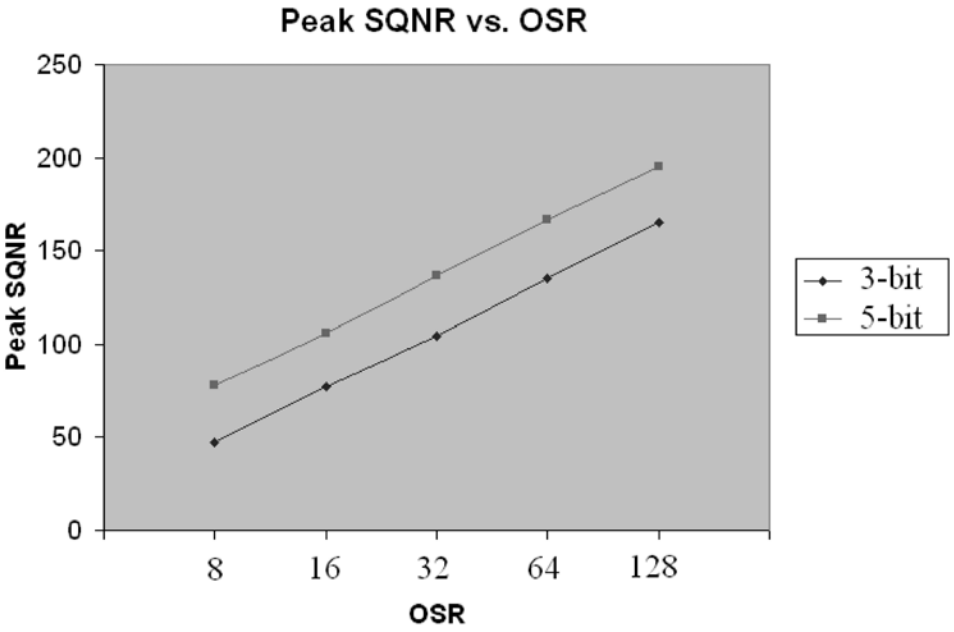

Fig. 17. Peak SQNR vs. OSR for fifth-order modulator

C. Design of the Prototype Modulator in System Level

1. Considerations for the Prototype Circuit Design

A main objective of this thesis is to make the theory practical in order to verify that this novel oversampling modulator can be implemented in a real circuit. We plan to develop a prototype circuit in 0.35-μm CMOS technology according to the system architecture in SIMULINK. As the first implementation, the complexity of the design is kept to a minimum. We aim to achieve high performance, in other words, wide bandwidth and high SNR (>80dB). This is done to demonstrate the practicality of the new oversampling modulation theory. We design the modulator in continuous-time because the original proposed oversampling modulation scheme is continuous-time. We choose the order of filter as three. For this proof-of-concept IC, a third order filter represents a non-trivial but lower complexity choice that can achieve high SQNR levels. We want to specify the signal bandwidth as high as possible. But for continuous-time modulators, it can be difficult to achieve a wide signal bandwidth (we explain this later). We choose 500kHz signal bandwidth as a conservative specification. To achieve a high SQNR, we choose OSR=32 and the internal quantizer resolution as 4-bit.

Thus, we'll design a prototype circuit of the NCO modulator in 0.35-μm CMOS technology as an OSR of 32, 3rd-order and 4-bit.

2. Simulation Results of Ideal Prototype Modulator

We build a 3rd-order 4-bit prototype oversampling modulator with an OSR of 32 in SIMULINK. In accordance with the design methodology discussed above, the parameters are adjusted to achieve the highest possible peak SQNR of the ideal oversampling modulator. The final parameters are:

- $f_s = 32e6$
- $N = 3$
- $R_p = 3$
- $R_s = 75$
- $shift = 8e6$
- $sat\_lim = 1$
- $nlevels = 16$
- $qi = (2 * sat\_lim)/nlevels$
- $k = 1.04 * abs(cm * bm) * qi$

Figure 18 shows the dynamic range of the modulator in SIMULINK.

We can see from the plot that peak SQNR is 101.1 when input is -5dB . Dynamic range is around 108dB.

3. Stability Discussion

For fixed OSR, filter order and number of quantizer bits, increasing Rs yields improved SNR. But we can not design the filter too aggressively. The system becomes unstable when Rs is too high. Figure 19 and Figure 20 show the stable case and unstable case. The upper part of the figure shows the time-domain behavior of conversion error, e_o in Figure 13. The lower part of the figure shows the time-domain behavior of quantizer input.

We can see the system becomes unstable when Rs, the minimum stop-band attenuation of the filter, increase from 68dB to 72dB. From above figures we can find

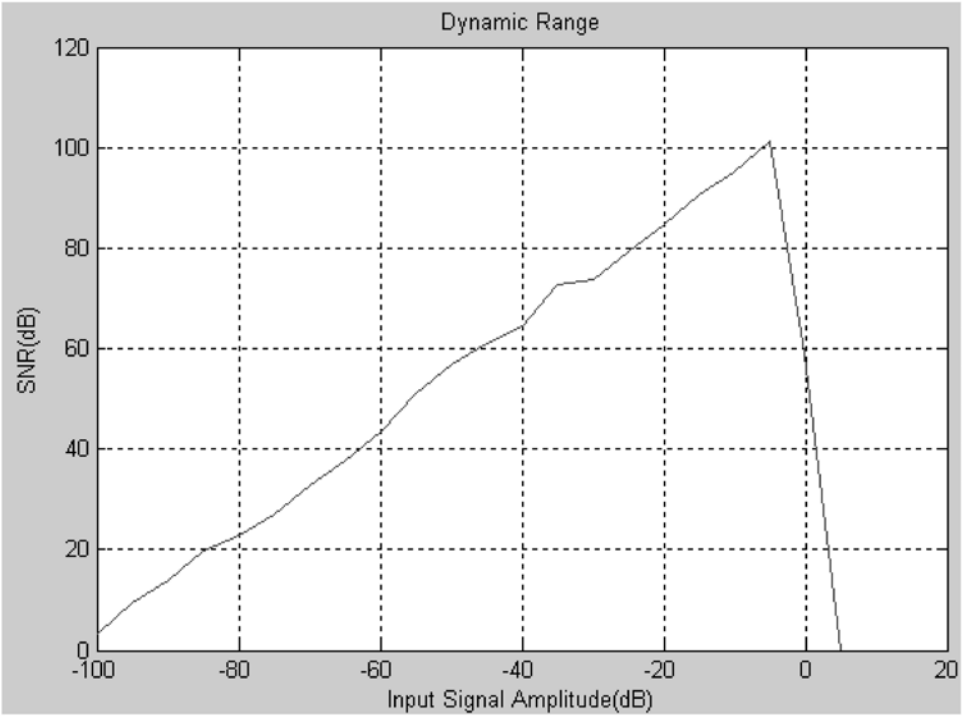

Fig. 18. Dynamic range of the ideal oversampling modulator

the conversion error, e_o, is very small (in the order of 10^{-4}) when the system is stable. It becomes more than ten thousand times larger when system becomes unstable. The same happens with the magnitude of the quantizer input.

We will introduce in a later section that the system would become unstable when the feedback loop delay is too large if the system is a continuous-time modulator.

4. Simulations for Effect of Non-Idealities

To do the simulations on effect of non-idealities, a new prototype modulator system in SIMULINK was created to introduce the errors on voltage references and delays of blocks.

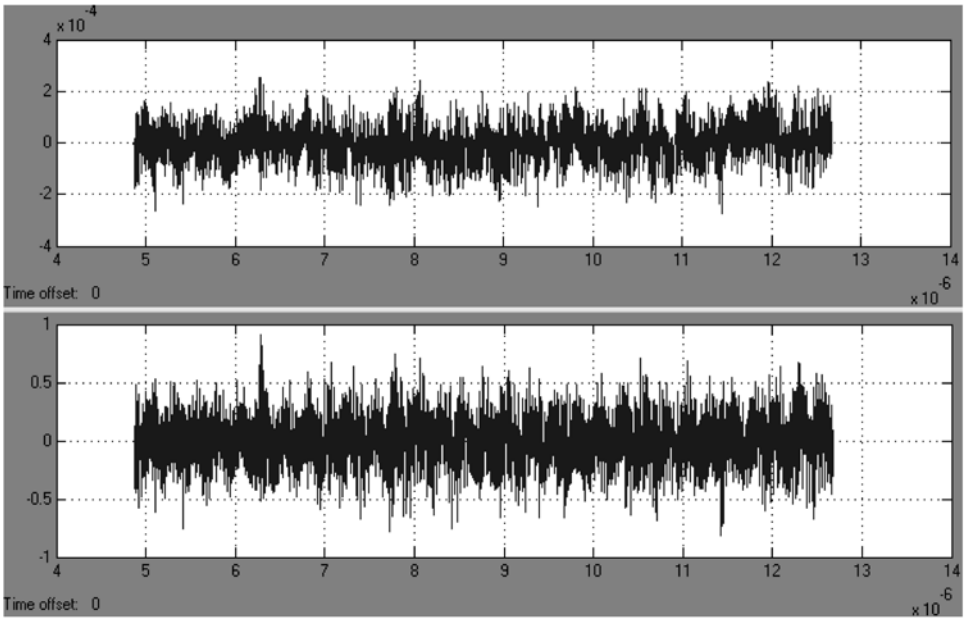

Fig. 19. Time domain behavior of system when OSR=8, N=5, nlevel=32, Rs=68dB

a. Errors on Voltage References

To introduce the errors on the voltage references, we use the function rand() in MATLAB to produce a 16*1 error vector which is added to the reference voltage of the quantizer.

For the ideal modulator, SQNR=99.7dB (input=-6dB). We performed several simulations using different random error vectors. The resulting SQNRs did not vary more than 3dB from ideal case. The results show that errors on voltage references should not affect the system too much.

b. Feedback Loop Delay

As shown in Figure 13, there are feedback loop delays which come from the sgn() block, internal ADC and DAC [15]. By simulation we find that non-zero feedback

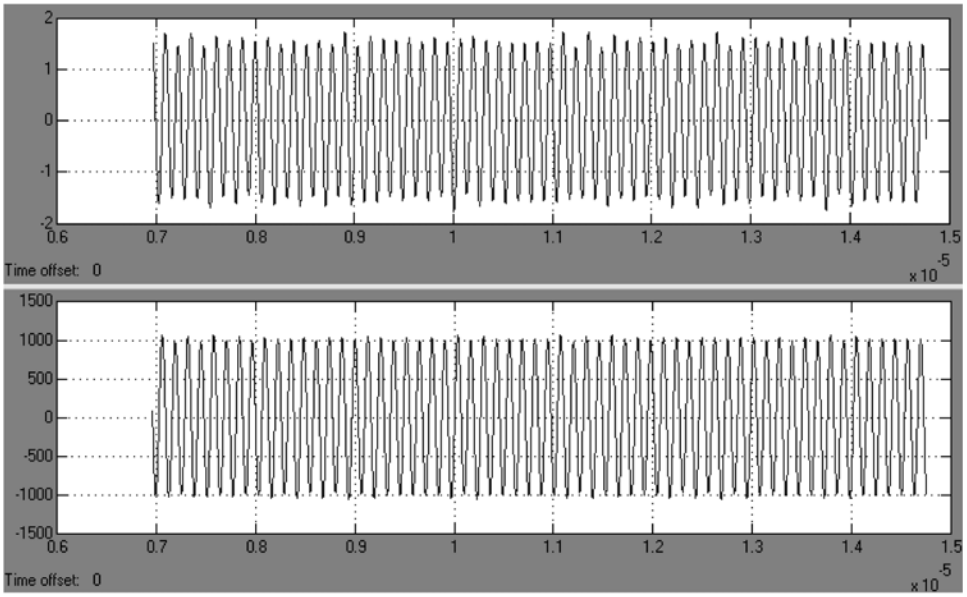

Fig. 20. Time domain behavior of system when OSR=8, N=5, nlevel=32, Rs=72dB

loop delay would degrade SQNR performance of the modulator or even cause the modulator to become unstable.

We did a series of simulations to study the effect of non-zero feedback loop delay on the system.

The setup is:

- $f_s = 32e6$
- $N = 3$
- $R_p = 2$
- $R_s = 72$
- $shift = 8e6$

Table I. Typical simulation data with different feedback loop delay(Rs=72, input=-6dB)

Delay	$0 * T_s$	$0.1 * T_s$	$0.14 * T_s$	$0.16 * T_s$
SQNR(dB)	94.5	92.6	85.0	65.4

- $sat\_lim = 1$
- $nlevels = 16$
- $qi = (2 * sat\_lim)/nlevels$
- $k = 1.04 * abs(cm * bm) * qi$
- Input = -6dB

We add a time delay block after the quantizer output. Then we do simulations to get SQNR. Data is shown in Table I.

Here $T_s = 1/f_s$.

The above data show that the performance of the modulator degrades when the feedback loop delay becomes large. The system even becomes unstable if the feedback loop delay is too large. Then we try to study if we can make the system be more tolerable to feedback loop delay. Finally we found that lower values of R_s of the filter can make the system more tolerable for non-zero feedback loop delay.

Consider the following data in Table II. Here, R_s equals 66dB. Other parameters are the same as last setup.

We find that a decrease in R_s makes the system more robust to non-zero feedback loop delay. But also we found that decreasing Rs 6dB results in the peak SQNR degrade for 2dB.

To simulate the system more realistically, a 5ns delay is introduced after the sgn() block. We decrease the R_s to 61dB. The simulation results are in Table III.

Table II. Typical simulation data with different feedback loop delay(Rs=66, input=-6dB)

Delay	$0 * T_s$	$0.1 * T_s$	$0.2 * T_s$	$0.3 * T_s$
SQNR(dB)	92.5	92.2	90.8	83.8

Table III. Typical simulation data with different feedback loop delay(Rs=61, input=-6dB)

Delay of quantizer	$0.0 * T_s$	$0.1 * T_s$	$0.2 * T_s$	$0.3 * T_s$	$0.4 * T_s$	$0.5 * T_s$
Delay of sign(ns)	0	5	5	5	5	5
SNR(dB)	90.2	86.4	84.7	84.2	81.9	79.2

Finally we get a proper filter design for the 3rd-order 4-bit prototype modulator. Please notice our design is very conservative because this is the first time that we implement this novel oversampling modulator. We leave a large safety margin, otherwise we can get better performance.

5. Ultimate System-Level Simulation Results of the Prototype Oversampling Modulator

The parameters are shown below:

- $f_s = 32e6$
- $N = 3$
- $R_p = 2$
- $R_s = 61$
- $shift = 8e6$
- $sat\_lim = 1$

- $nlevels = 16$
- $qi = (2 * sat\_lim)/nlevels$
- $k = 1.04 * abs(cm * bm) * qi$

Figure 21 shows the dynamic range of the modulator in SIMULINK.

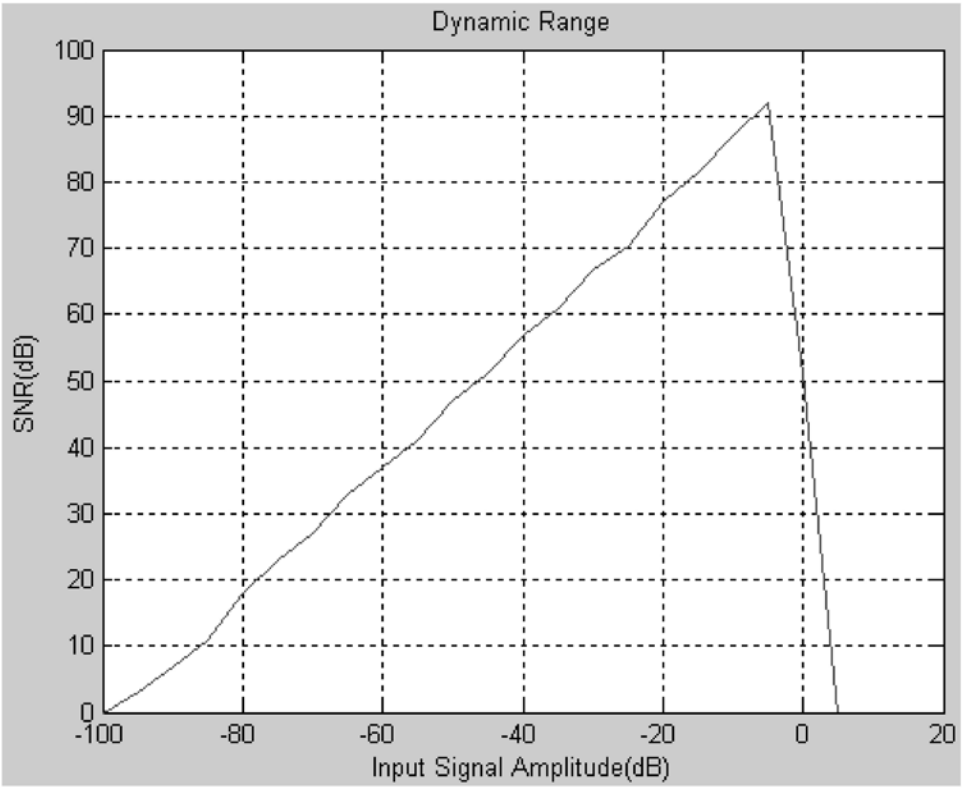

Fig. 21. Dynamic range of the prototype oversampling modulator

The above plot shows that peak SNR is 92 when input is -5dB. Dynamic range is around 99dB.

CHAPTER V

CIRCUIT DESIGN AND IMPLEMENTATION

This chapter describes the circuit-level design of the prototype third-order four-bit continuous-time NCO modulator. This design is implemented in a 0.35-μm double-poly CMOS technology (TSMC35_P2) from TSMC. Fully differential structure is used to maximize noise rejection and increasing dynamic range [16].

Based on the system-level simulation results, the preliminary design specifications of this research are shown in Table IV.

A. Building Blocks

According to the block diagram of the NCO modulator, which is shown in Figure 13, we divide the circuits into a number of building blocks, including filter, controller, internal ADC, DAC, DAC current calibration and clock generation circuit [17] [18] [19] [20].

The block diagram of the prototype NCO modulator in circuit-level is shown in Figure 22.

B. Third-Order Continuous-Time Filter

The filter block is illustrated in Figure 23. The two inputs are input analog signal and current feedback from DAC. Outputs are conversion error, e_o, and state outputs of the filter, e_1, e_2, e_3. All inputs and outputs are fully differential signals. According to the requirements of the filter in system-level, our main considerations are:

1. It is a third-order continuous-time filter.

2. It has two inputs: the input analog voltage and feedback current from internal

Table IV. Preliminary design specifications of this research

Signal Bandwidth	500KHz
Sampling Frequency	32MHz
OSR	32
Dynamic Range	>84dB
Supply Voltage	±1.65V
Power Consumption	< 200mW
Area	< 3mm*3mm
Process	0.35-μm CMOS (TSMC35_P2)

DAC, and four voltage outputs: the conversion error, e_o, and state outputs, e_1, e_2 and e_3.

3. This structure should be able to realize arbitrary zeros and poles of the filter.

4. High linearity and high SNR.

5. Low cost. In other words, lessen the number of opamps used in this filter.

6. Robust to process variation.

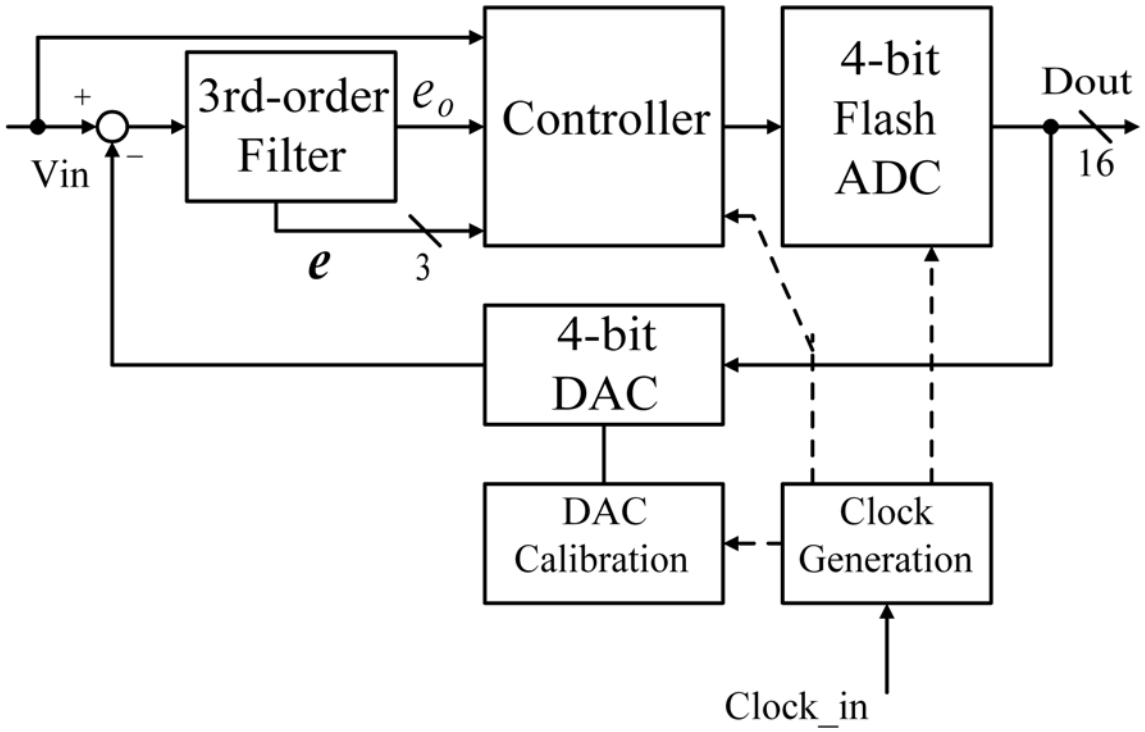

Fig. 22. Block diagram of the prototype NCO modulator in circuit-level

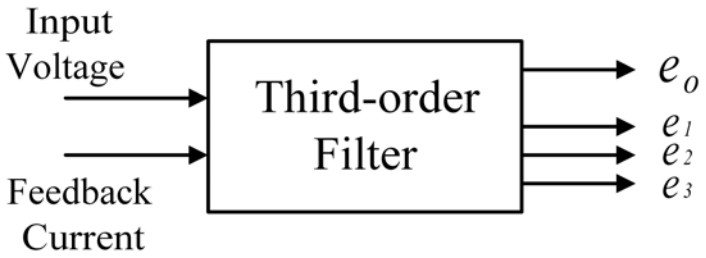

Fig. 23. Third-order filter block

Table V. Comparison of filter structures

	Cascade	Leapfrog	FLF
Opamps needed	Fewer	More	More
Sensitivity	High	Low	Medium
Tunability	Easy	Difficult	Easy

1. Proposed Structure

After studying many filters [21] [22] [23], we decide to choose the FLF (Follow the Leader Feedback) structure [24] [25]. The optimized FLF design has been shown to be the most practical multiple-loop feedback design based on sensitivity, dynamic range, and noise performance [22] [26].

It can fulfill all the requirements we list above. Another advantage of the FLF filter is that it is easy to tune. Table V shows a comparison between the most popular structures, cascade connection of second-order sections, Leapfrog and FLF.

The third-order FLF filter topology is shown in Figure 24. The transfer function of the FLF filter is [22]:

$$\begin{aligned} H(s) &= K_0 \frac{B_0(s+k)^3 + B_1 k(s+k)^2 + B_2 k^2(s+k) + B_3^3}{(s+k)^3 + F_2 k^2(s+k) + F_3 k^3} \\ &= K_0 \frac{B_1 k s^2 + (2B_1 k + B_2 k^2)s + (B_1 + B_2 + B_3)k^3}{s^3 + 3ks^2 + (3k^2 + F_2 k^2)s + (1 + F_2 + F_3)k^3} \end{aligned} \tag{5.1}$$

Here $B_0 = 0, K_1 = K_2 = K_3 = 1$.

Eq. (5.1) shows for a filter with given arbitrary zeros and poles, we can realize it by the FLF structure.

From the FLF filter topology, we get the state-space matrix of the filter shown below. Here we define the nodes voltage, e_1, e_2, e_3, as state outputs.

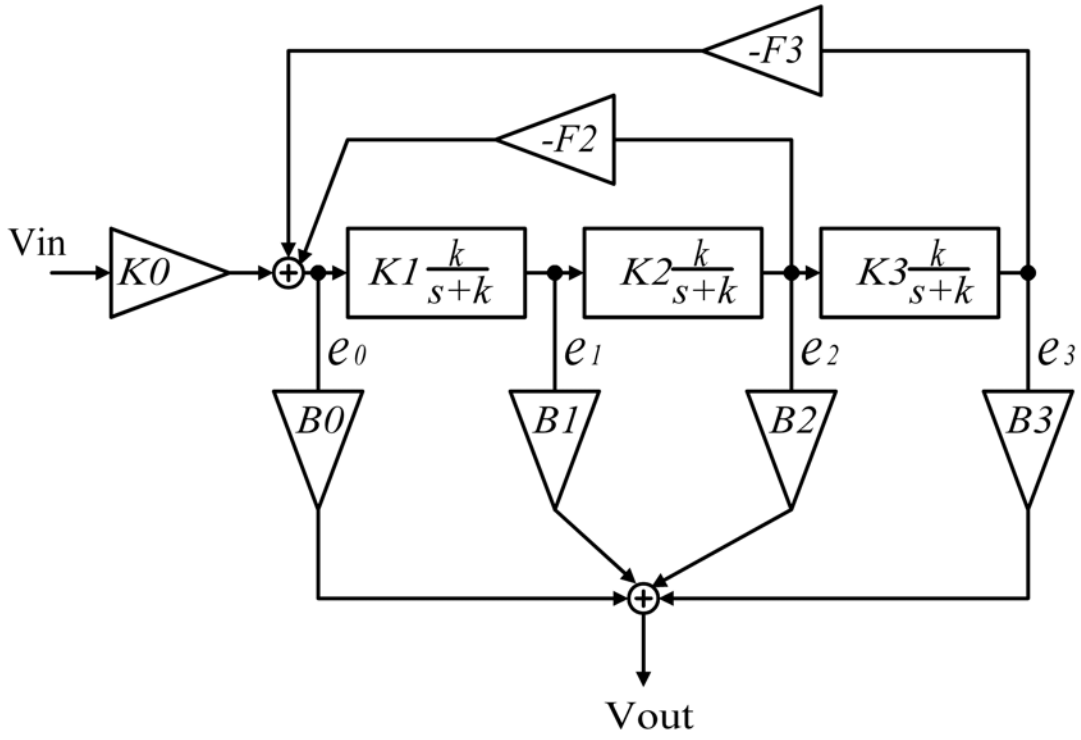

Fig. 24. The third-order FLF filter topology

$$\dot{e}_3 = -ke_3 + K_3 ke_2 \tag{5.2}$$

$$\dot{e}_2 = -ke_2 + K_2 ke_1 \tag{5.3}$$

$$\dot{e}_1 = -ke_1 + K_1 ke_0 \tag{5.4}$$

$$e_0 = K_0 V_{in} - F_3 e_3 - F_2 e_2 \tag{5.5}$$

From the above equations we deduce that:

$$\begin{bmatrix} \dot{e}_3 \\ \dot{e}_2 \\ \dot{e}_1 \end{bmatrix} = \begin{bmatrix} -k & K_3k & 0 \\ 0 & -k & K_2k \\ -F_3K_1k & -F_2K_1k & -k \end{bmatrix} \begin{bmatrix} e_3 \\ e_2 \\ e_1 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} K_0K_1kV_{in} \tag{5.6}$$

$$V_{out} = \begin{bmatrix} B_3 & B_2 & B_1 \end{bmatrix} \begin{bmatrix} e_3 \\ e_2 \\ e_1 \end{bmatrix} \tag{5.7}$$

where $B_0 = 0$.

The matrices obtained would be used to design the controller.

2. The Maximizing of Filter Dynamic Range

To reduce noise in the filter circuit, we need to maximize dynamic range of each stage of filter. In Eq. (5.1) we assume $K_1 = K_2 = K_3 = 1$. To maximize dynamic range, the gain of the filter, K_0, is distributed to the gain of each stage, k_1, k_2, k_3. Thus the signal amplitude at the output of each stage have equal maximum value.

The transfer function of the third stage of the filter is

$$H_3(s) = K_0 \frac{s^3}{s^3 + 3ks^2 + (3k^2 + F_2k^2)s + (1 + F_2 + F_3)k^3}. \tag{5.8}$$

Let $a = \frac{k}{s+k}$. Then the transfer function of each stage is:

$H_2(s) = \frac{H_3(s)}{a}$

$H_1(s) = \frac{H_2(s)}{a}$

$H_0(s) = \frac{H_1(s)}{a}$

From the BODE simulation in MATLAB, the frequency response spectrum of each stage is obtained. And the maximum gain of each stage is obtained as:

$V_{o,max} = max(|H(s)|)$

$V_{3,max} = max(|H_3(s)|)$

$V_{2,max} = max(|H_2(s)|)$

$V_{1,max} = max(|H_1(s)|)$

$V_{0,max} = max(|H_0(s)|)$

K_1, K_2 and K_3 are obtained by the relations:

$K_1 = \frac{V_{0,max}}{V_{1,max}}$

$K_2 = \frac{V_{1,max}}{V_{2,max}}$

$K_3 = \frac{V_{2,max}}{V_{3,max}}$

This implies the feedback and feed-forward coefficients should be readjusted as:

$F_2' = F_2/K_1K_2$

$F_3' = F_3/K_1K_2K_3$

$B_1' = B_1K_2K_3$

$B_2' = B_2K_3$

$B_3' = B_3$

3. Parameter Calculation

The power supply voltage used is 3.3V. Considering the maximum signal swing and circuit design, the full scale of the signal is defined as ±600mV (0dB signal).

On simulating in system-level, we observe that the magnitude of the output of the filter is small, approximately 10^{-4}V. That would make the design of sgn() block (shown in Figure 13) difficult. To solve this problem, a gain of 200 is introduced to the filter. First, we get original transfer function of the filter from system-level design.

$$H(s) = \frac{3.065 * 10^4 s^2 + 4.904 * 10^{11} s + 1.032 * 10^{19}}{s^3 + 2.313 * 10^6 s^2 + 1.012 * 10^{13} s + 1.032 * 10^{19}} \tag{5.9}$$

Zeros and Poles of the filter are:

Zeros=

$-8.0000 * 10^6 + 1.6516 * 10^7 i$

$-8.0000 * 10^6 - 1.6516 * 10^7 i$

Poles=

$-5.6868 * 10^5 + 2.9087 * 10^6 i$

$-5.6868 * 10^5 - 2.9087 * 10^6 i$

$-1.1752 * 10^6$

Equating the transfer functions shown in Eq. (5.1) and Eq. (5.9), all the coefficients are calculated. The dynamic range is then maximized. The results are:

$k = 7.71 * 10^5$

$K_1 = 20$

$K_2 = 20$

$K_3 = 4$

$F_2 = 0.70122$

$F_3 = 0.093662$

$B_1 = 3.9754 * 10^{-1}$

$B_2 = 3.7273 * 10^{-1}$

$B_3 = 2.7165$

Figure 25 shows the frequency response spectrum of the filter. Please note that in this figure, the gain of the filter is divided by 200 to make the observation more clear.

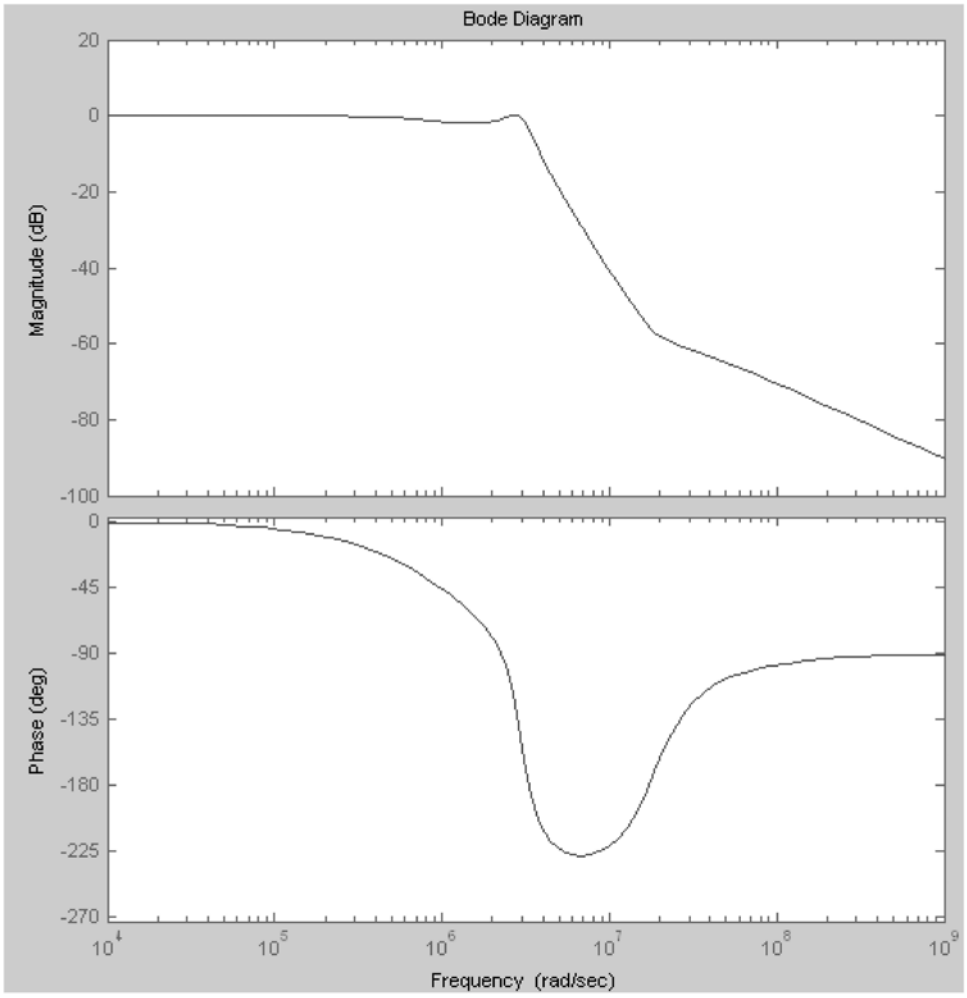

Fig. 25. Frequency response spectrum of the filter

Table VI. The SQNR performance under time constant variations (input=-6dB)

RC time constant Variation	SQNR(dB)
0	90.2
+10%	88.1
-10%	90.2
+20%	89.3
-20%	86.0

4. Effect of Time Constant Variation in the Filter

Simulations are performed to see how much the variation will affect the performance. The RC time constant, k, of each stage of the filter is changed in system model in SIMULINK. And simulations are run to get the SQNR performance of the modulator system. The results are shown in Table VI.

From the simulation data we can see that the FLF filter is quite robust for the time constant variation in the system.

5. Schematic of the Filter

In this section we will describe the schematic design of the filter.

To realize the integrator in the filter, two popular structures are considered: active-RC and Gm-C integrator, as shown in Figure 26 and Figure 27.

Active-RC structure is choosen for the reasons detailed below:

1. It has higher close-loop linearity.
2. It has larger output swing.
3. The virtual ground of the opamp is ideal as a current feedback point for the feedback DAC.

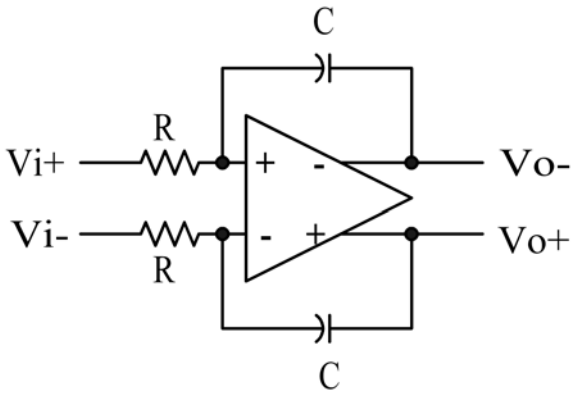

Fig. 26. Active-RC integrator circuit structures

Based on block diagram of the filter shown in Figure 24, the fully differential third-order continuous-time filter circuit is design as shown in Figure 28.

The components values are calculated as follows:

Let $C = 50\text{pF}$

Then $R = 1/k * C = 25.94\text{k}$

$R1 = R/K_1 = 1.297\text{k}$

$R2 = R/K_2 = 1.297\text{k}$

$R3 = R/K_3 = 6.485\text{k}$

$RF2 = R/F_2 = 36.992\text{k}$

For $RF3$, here is a trick. As the above method, the value of $RF3$ should be calculated as $RF3 = R/F_3 = 276.953\text{k}$. It's too large compared with other transistors, thus difficult for layout. Two additional resistors are used to split the coefficient F_3 as $0.1 * 0.93662$. Thus $RF3 = R/0.93662 = 27.695\text{k}$. To get the coefficient 0.1, the value of R8 and R9 are chosen as 0.2k and 1.8k.

Let $R7 = 3\text{k}$

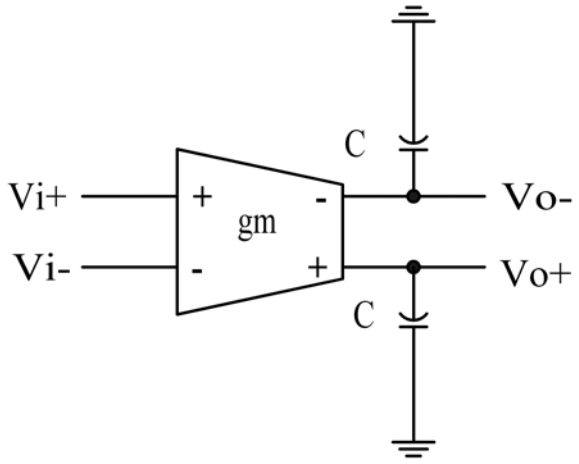

Fig. 27. Gm-C integrator circuit structures

Then $R4 = R7/B_1 = 7.546\text{k}$

$R5 = R7/B_2 = 8.048\text{k}$

$R6 = R7/B_3 = 1.104\text{k}$

In Figure 28 it is observed that four stages are used in the filter. The first three stages correspond to the three stage first-order integrators in Figure 24. The last stage is the summer stage. Two kinds of opamps are used here. Opamp2 is used in integrator stages. Opamp1 is used in summer stage. We'll introduce these two opamps in the next section.

In Figure 28 the adjustable capacitor C is realized by a capacitor bank for filter tuning. The RC time constant varies around 30% under the TSMC 0.35μm technology in fabrication. Although the FLF filter is robust for the process variation, the RC time constant tuning circuit is used in the design to ensure the high performance of the system in worst case.

In the filter, $vi\pm$ is the input analog signal. Ii is the feedback current from

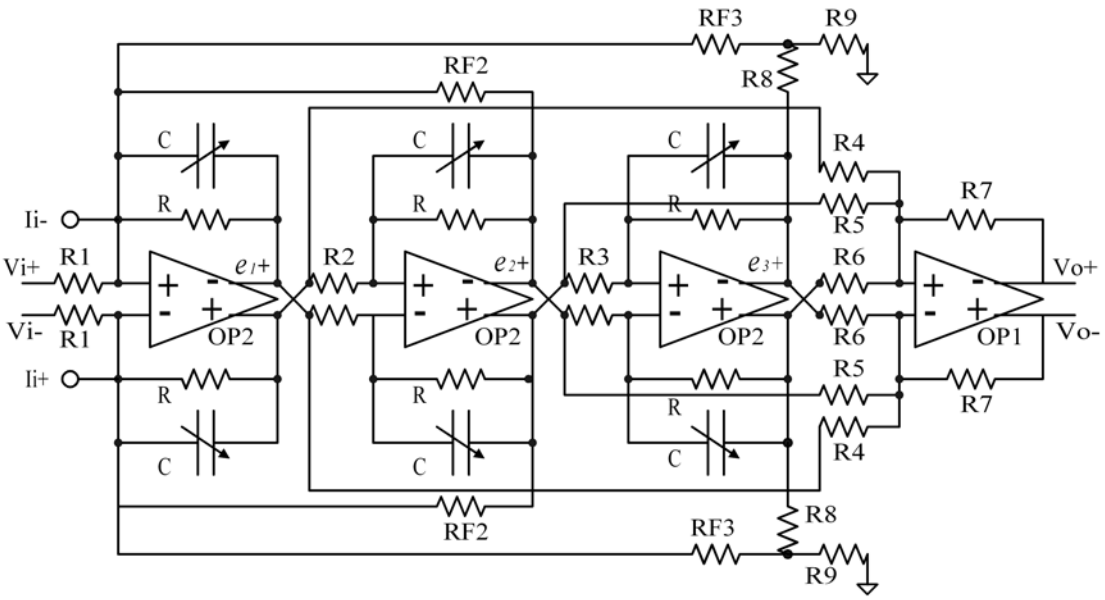

Fig. 28. Schematic of the fully-differential third-order continuous-time FLF filter

DAC. The four inputs, *tune*_1, *tune*_2, *tune*_3, and *tune*_4, are control signals for the capacitor bank. There are four pairs of output. $vo\pm$ is output voltage of the filter. $x1$, $x2$ and $x3$ are status output voltages of the filter.

The AC analysis of the filter is performed in Cadence and the frequency response plot is obtained as shown in Figure 29. As compared with the frequency response plot shown in Figure 25 which is from MATLAB simulation, it is observed that they are almost the same.

6. Opamps

There are two kinds of opamps in the filter. Opamp1 is used in the summer stage. Opamp2 is used in all integrator stages. For the summer stage, the main requirement is that the settling time should be short. Thus a high GBW and high slew rate for

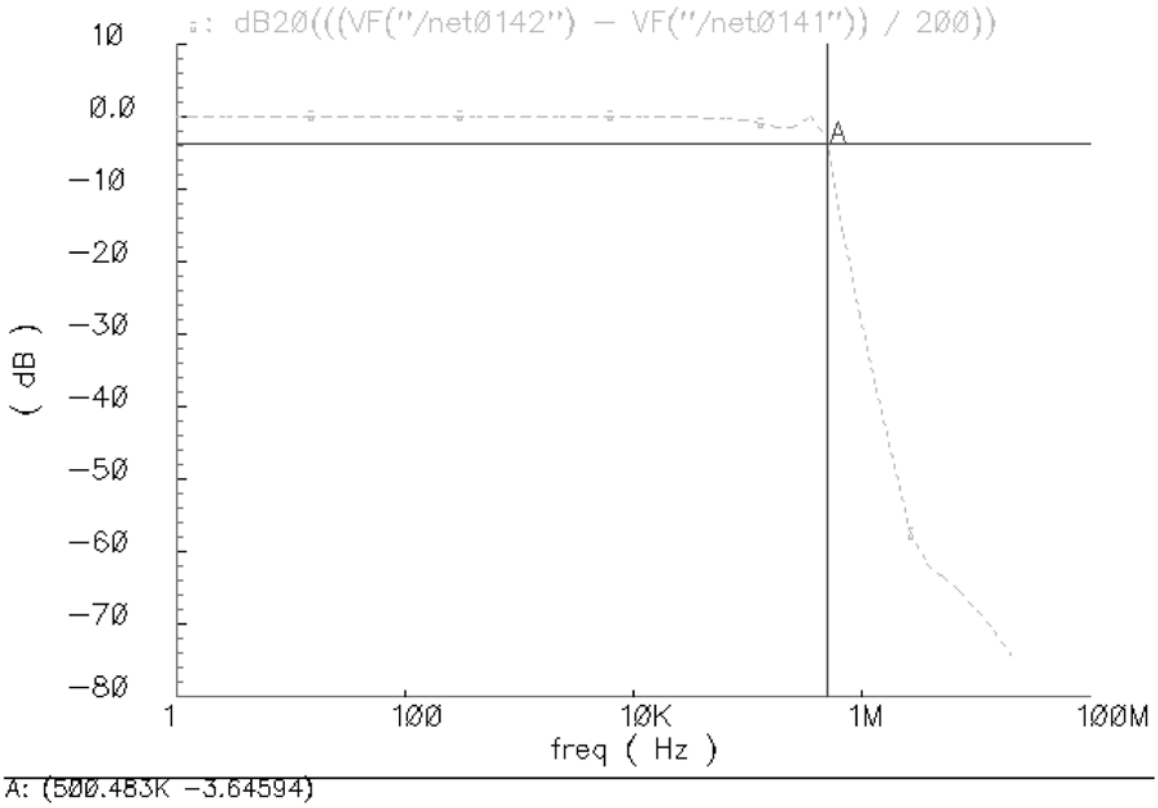

Fig. 29. Frequency response spectrum of the filter

Opamp1 is needed.

For integrator stages, a high DC gain for Opamp2 is needed to get high close-loop linearity.

The specifications of Opamp1 and Opamp2 are shown in Table VII.

A typical two-stage opamp structure employing Miller compensation is choosen for both Opamp1 and Opamp2 [16]. The topology of the opamp is shown in Figure 30. The transistor sizes of Opamp1 are given in Table VIII. The transistor sizes of Opamp2 are given in Table IX.

Usually there is a buffer stage in the opamp to drive the resistance load. By

Table VII. Specifications of Opamp1 and Opamp2

	Opamp1	Opamp2
DC gain(dB)	50	55
GBW(MHz)	500	40
PM(degree)	70	70
Slew Rate(V/s)	$5 * 10^9$	10^8

Table VIII. Transistor sizes of Opamp1

Transistors	Size m(W/L) (μm)
M0, M9	10(18/0.6)
M1, M2, M10, M11	10(12/0.6)
M3, M4, M12, M13	5(6/0.6)
M5, M6	10(18/0.6)
M7, M8	10(6/0.6)

Table IX. Transistor sizes of Opamp2

Transistors	Size m(W/L) (μm)
M0, M9	20(14/2)
M1, M2, M10, M11	10(4.1/2)
M3, M4, M12, M13	10(7/2)
M5, M6	30(18/0.4)
M7, M8	30(9/0.4)

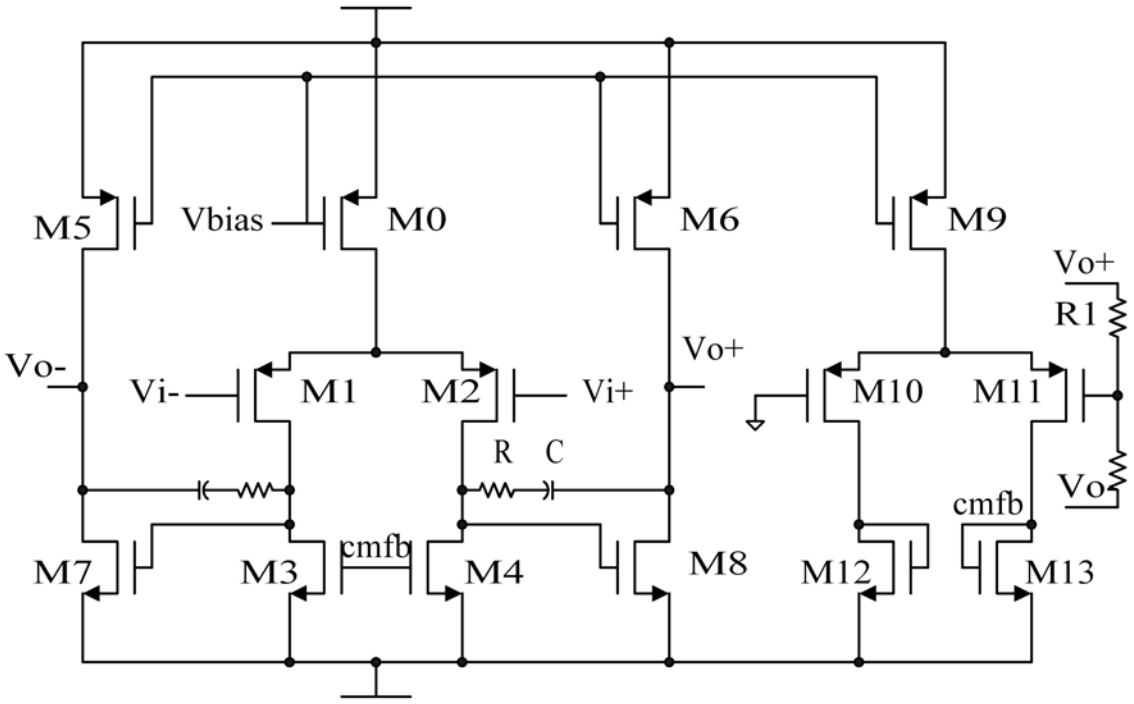

Fig. 30. Schematic of the opamp

simulations it's observed that the buffer stage needs a lot of current and restricts the output swing. Hence this stage is removed. To keep the open loop gain without buffer, the resistance load is carefully designed to be large enough for every opamp used in the system.

We can see a differential OTA stage in the right of Figure 30. That is the common-mode feedback circuit. It's necessary for the fully differential opamps. In this system the supply voltage is ±1.65V. The common-mode output voltage is set as 0V.

Table X shows the Cadence simulation results for the two opamps. When we do the simulations, the load of Opamp1 is 2KΩ resistance. The load of Opamp2 is 50pF capacitance//1KΩ resistance. .

Table X. Cadence simulation results for Opamp1 and Opamp2

	Opamp1	Opamp2
DC gain(dB)	49	55.8
GBW(MHz)	540	41
PM(degree)	70	78
Slew Rate(V/s)	$5.1 * 10^9$	$1.1 * 10^8$
Power Consumption(mW)	10.8	11.1

C. Controller

The circuit-level implementation of the controller is shown in Figure 31. An opamp and resistors are used instead of the gain and sum blocks in Figure 13.

1. Comparator

Figure 32 shows the block diagram of the sgn() block. It is divided into three parts.

The comparator part is to compare the input differential signal and generate the digital output.

The synchronization latch part synchronizes the digital output. When the input signal of the comparator is very small, the regeneration time of the comparator will be quite long and uncertain. This phenomenon is called "metastability" [27] [28]. The synchronization latch circuit is necessary to eliminate the effect of metastability. The schematic of the synchronization latch circuit is shown in Figure 33. In this figure, $clk3$ is the clock to synchronize the digital output. *calib_ctr* is the control signal to forbid the digital output during the DAC calibration.

The output of the comparator would be added to the output by a coefficient k. This function is realized by the 1-bit DAC circuit. The schematic of the 1-bit DAC

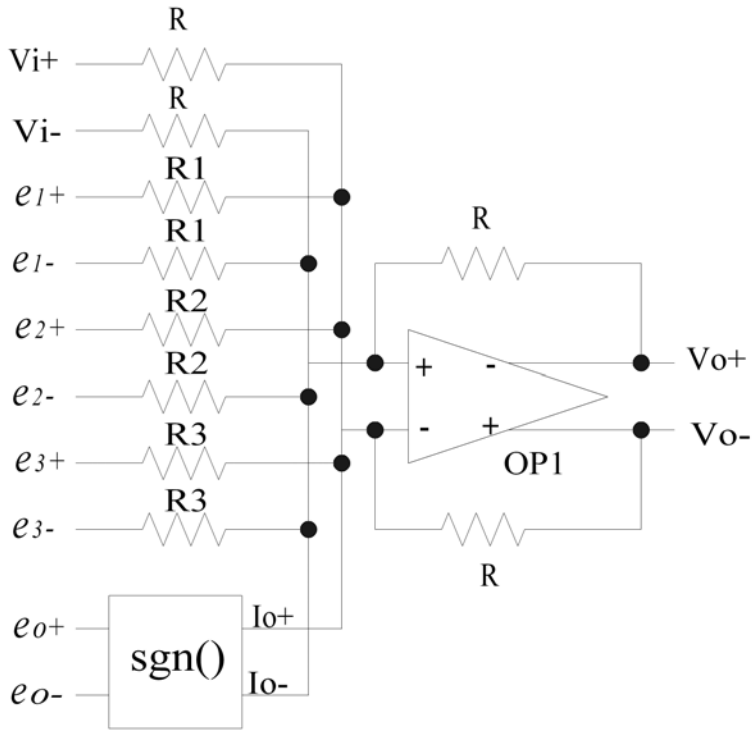

Fig. 31. Schematic of the controller

is shown in Figure 34.

The comparator block is a crucial block in the system. It is necessary to minimize the delay of the comparator as much as possible. Large feedback loop delay degrades the performance of the modulator, even causes the modulator to become unstable.

For the sgn() block, the accuracy is also important. Thus we need design a high-speed comparator with reasonable accuracy.

The comparator circuit consists of a differential pair, a track-and-latch stage and an S-R latch. The schematic of the comparator is shown in Figure 35 [28] [29].

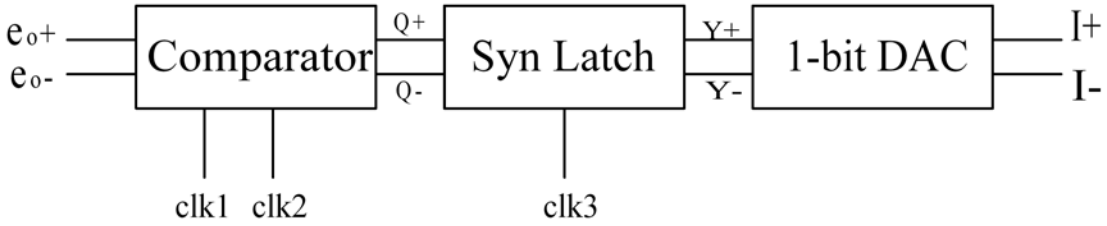

Fig. 32. Block diagram of the sgn() block

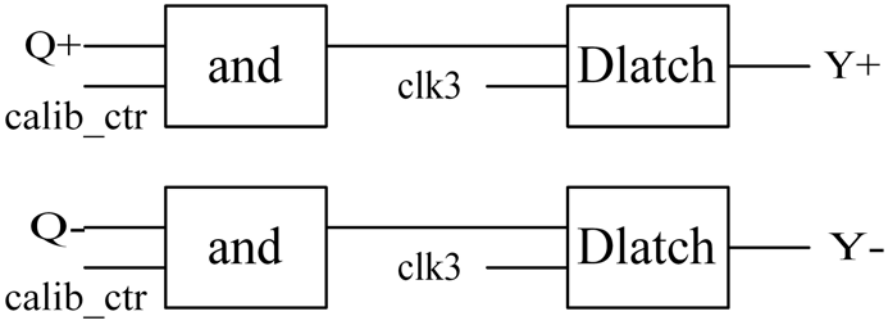

Fig. 33. Schematic of the synchronization latch circuit

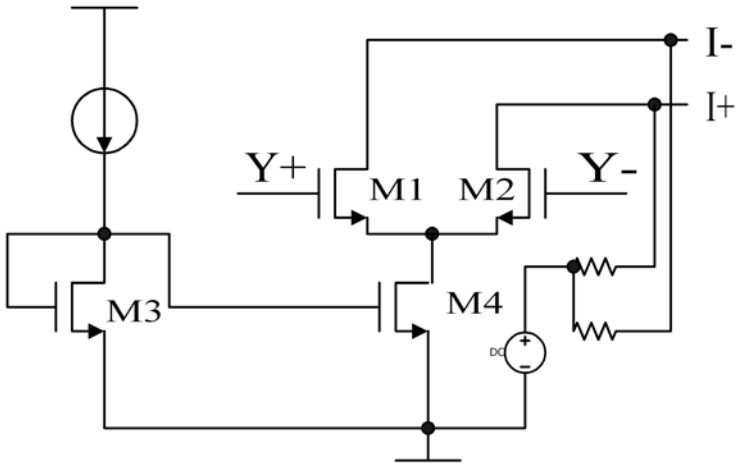

Fig. 34. Schematic of the 1-bit DAC

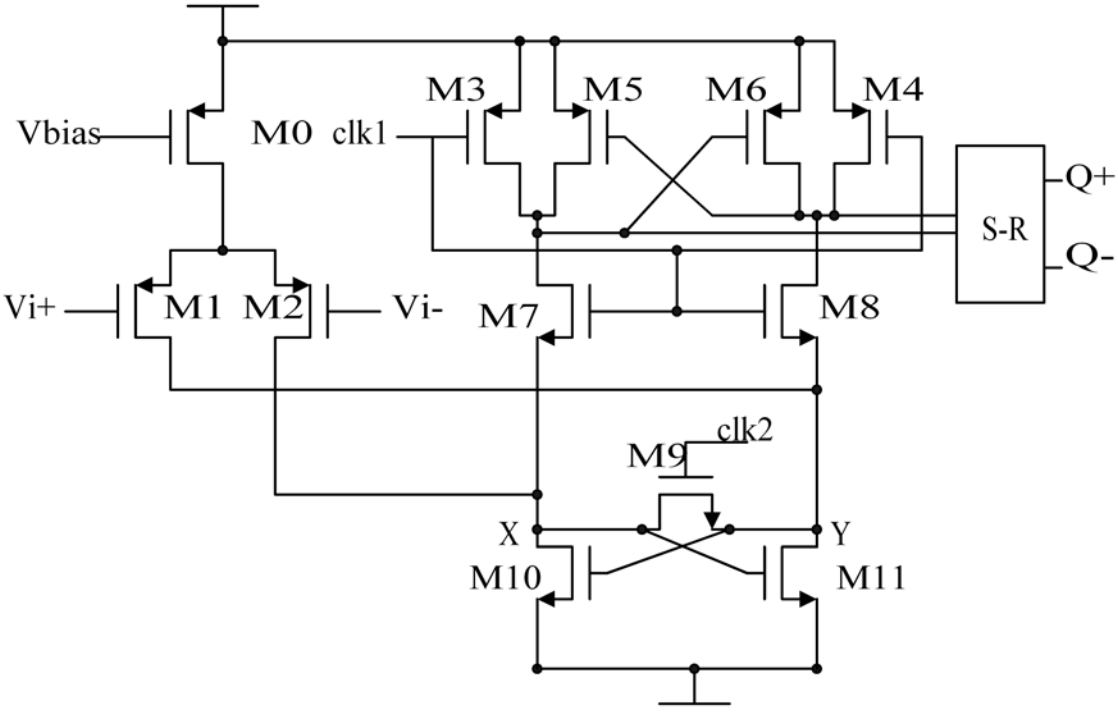

Fig. 35. Schematic of the comparator

Table XI. Transistor sizes of the comparator in sgn() block

Transistors	Size m(W/L) (μm)
M0	2(4.5/0.4)
M1, M2	3(2.4/0.4)
M3, M4	2(1.5/0.4)
M5, M6	2(4.5/0.4)
M7, M8	1(1.2/0.4)
M9	1(1.2/0.4)
M10, M11	1(3.6/0.4)

The transistor sizes of the comparator are given in Table XI.

The comparator operates in two phases: tracking phase and latch phase. In track phase, clk1=low and clk2=high. $M9$ is on and the upper half of second stage is off. The input voltage is amplified and appears on point X and Y. In the same phase, $M3$ and $M4$ pull the output to VDD.

The voltage between X and Y is [29]:

$$V = \frac{g_{m0,1}R_{on,19}}{2 - g_{m15,16}R_{on,19}}V_{in} \tag{5.10}$$

In latch mode, clk1=high and clk2=low. $M9$ is off. $M7$, $M8$ are on. The regeneration due to positive feedback takes place. The voltage V is soon amplified to a voltage swing nearly equal to the power supply voltages.

For proper operation, clk1 and clk2 are complementary. But it is important that clk2 turns off $M9$ before clk1 turns on $M7$ and $M8$. The clock phases are shown in Figure 36. Topology of the circuit generating clk1 and clk2 is shown in Figure 37.

To optimize the comparator to operate at maximum comparison speed, minimum channel length transistors should be used, and the following ratio between widths W

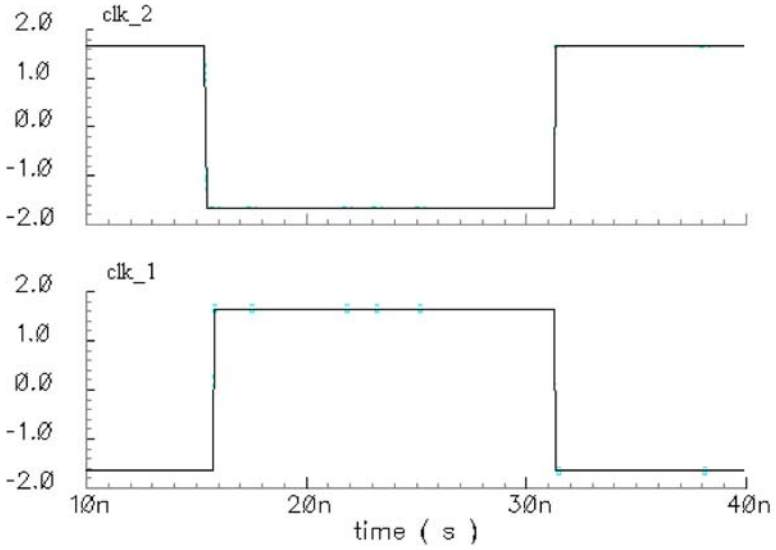

Fig. 36. Clock phases of clk1 and clk2

is recommended [29].

$W19 = \frac{1}{3}W15$

$W1 = 2W15$

$W13 = W19$

$W9 = 2.5W19$

$W10 = 2.5W15$

The comparator is simulated with a SR-latch load. Simulations show the resolution of the comparator is 75μV. The regeneration time is 0.7ns (90% accuracy). Meets the requirements.

D. 4-bit Internal Flash ADC

We design a 4-bit internal flash ADC to work as the quantizer in system-level design [30] [31] [32] [33]. The diagram of the flash ADC is shown in Figure 38.

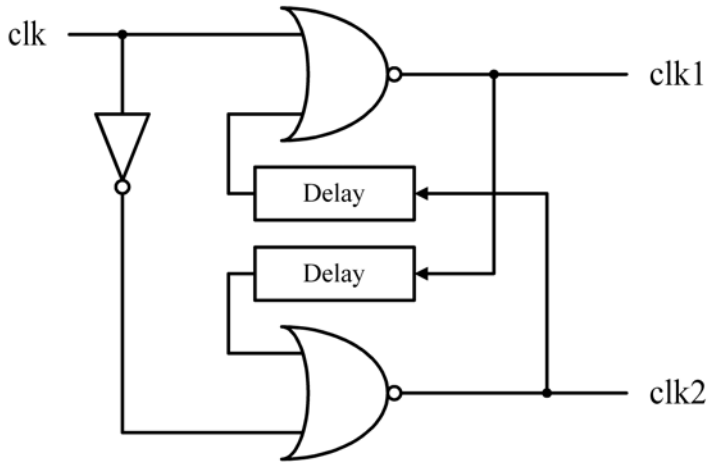

Fig. 37. Topology of the clock generation circuit

We choose flash topology because of its high speed, which means that the feedback loop delay would be quite small. The resolution requirement is only 4-bit, quite suitable for flash ADC [28]. Below are the main considerations when we design the flash ADC:

1. Speed. It should work as fast as possible with acceptable power consumption.

2. The whole input capacitive loading of the flash ADC must be minimized. There are 16 comparators parallel connected in the 4-bit ADC. So it's important to carefully design the input stage of the comparator otherwise the large input parasitic capacitance would limit the speed of the comparator and usually requires a strong and power-hungry buffer to drive it.

3. Minimal power consumption.

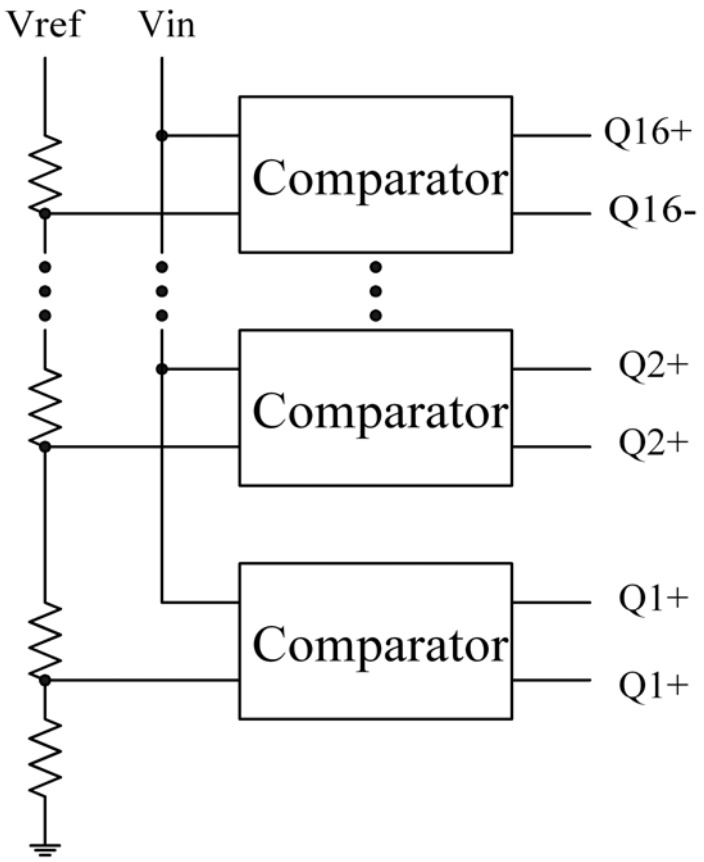

Fig. 38. Diagram of the flash ADC

Figure 39 shows the detailed schematic of the comparator block in the flash ADC. It is similar to the comparator in sgn() block. But there are also some differences:

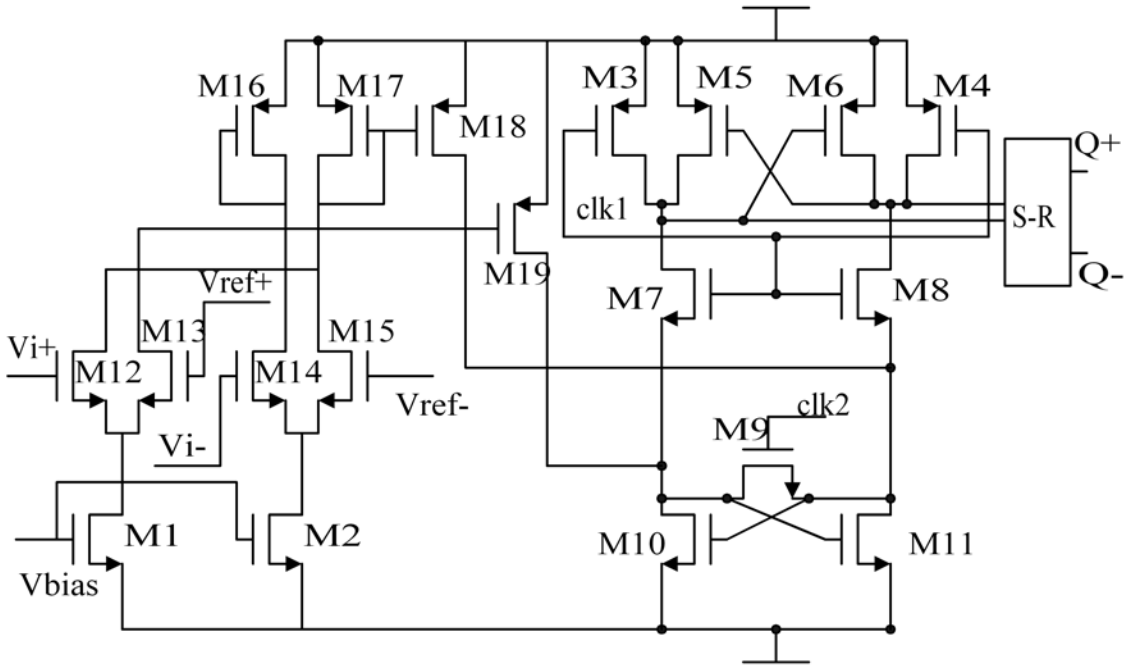

Fig. 39. Schematic of the comparator block in the flash ADC

Two fully differential pairs are used as the input stage for the fully differential input and voltage reference. The NMOS input gates are used instead of PMOS input gate in comparator in "sgn()" block. This arrangement minimize the size of input devices thus minimize the input parasitic loading. It is a well known fact that to get a given transconductance, the size of PMOS transistor should be three times of the size of NMOS transistor. PMOS current mirrors ($M16$, $M17$, $M18$, $M19$) are used to provide both gain and isolation from latch stage, to reduce kick-back noise.

Table XII. Transistor sizes of the comparator in the flash ADC

Transistors	Size m(W/L) (μm)
M1, M2	2(1.5/0.4)
M12, M13, M14, M15	1(2/0.4)
M16, M17	3(2/0.4)
M18, M19	3(3/0.4)
M3, M4	1(2.5/0.4)
M5, M6	1(7.5/0.4)
M7, M8	1(1/0.4)
M9	1(1/0.4)
M10, M11	1(3/0.4)

The transistor sizes of the comparator are given in Table XII. The comparator is simulated with a SR-latch load. Simulations show the resolution of the comparator is 210μV. The regeneration time is 0.7ns (90% accuracy). Meets the requirements.

Please notice there is also a synchronization latch after a comparator. It's more important here to add this block, because there are 16 comparators in the 4-bit flash ADC. The large glitch would exist on the output of the ADC without the synchronization latches. Simulations show the SQNR performance degrades 5dB without the synchronization latches.

There is a delay between the synchronization clock used in flash ADC and the synchronization clock used in sgn() block. That is because a short settling time is needed when the output current of the 1-bit DAC in sgn() block is added on the sum block before the flash ADC.

E. 4-bit DAC and Current Calibration Circuit

1. 4-bit DAC

The current-steering architecture is chosen for the DAC design because it's the most suitable candidate for high-speed operation. The reason is current-steering DAC can drive resistive loads directly. It doesn't require high-speed opamp at the output and hence is potentially faster than other types of DACs [28]. Another advantage of current-steering DAC is the convenience to interface the DAC output current with the continuous-time filter.

The DAC structure diagram is shown in Figure 40. There are 16 binary weighted

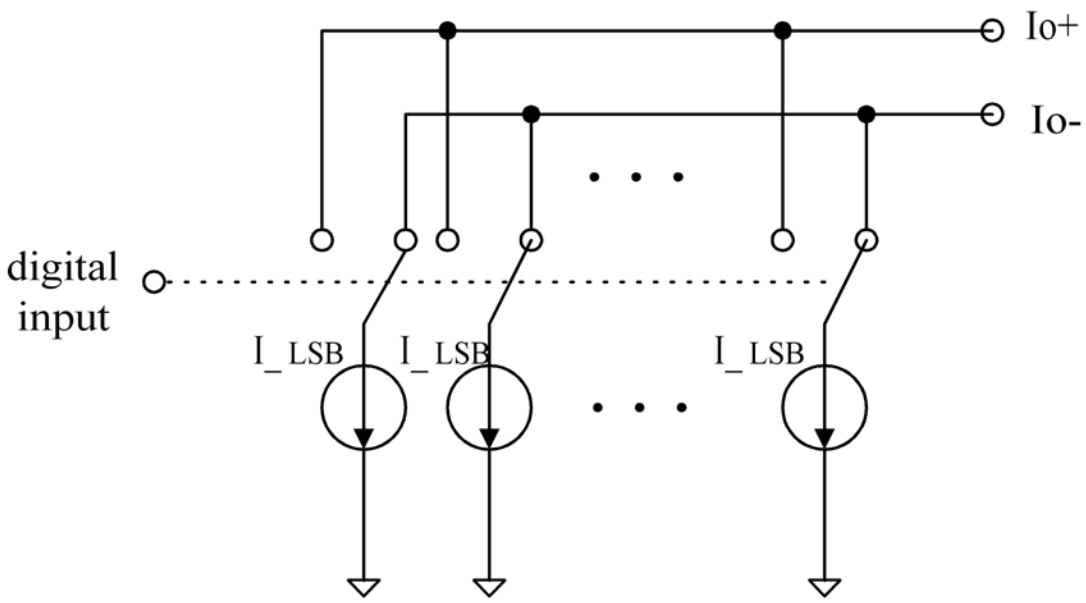

Fig. 40. DAC structure diagram

current sources and 16 switches. The switches are dependent on the digital input, and they determine which current source should be directed to which output.

Figure 41 shows the schematic of an unit current source. The unit current source

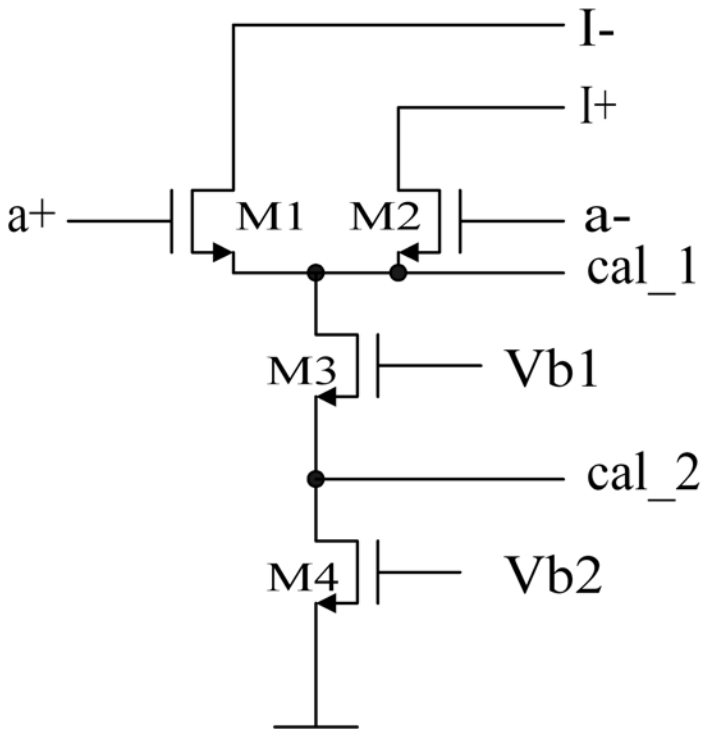

Fig. 41. Schematic of an unit current source

consists of two cascode NMOS transistors. The cascode structure is used to increase output impedance.

Differential switches are used so that the current source can always deliver current. Otherwise if the current source is turned off, the voltage at the output of current source will move to the supply voltage. When the current source is turned on again,

the voltage between the output of current source and the DAC output would be large. This will cause big glitch [34].

In Figure 41 the input cal_1 and cal_2 are used for current calibration. We'll introduce it in next section.

2. Current Calibration Circuit

We need to consider the linearity problem of the multi-bit internal DAC. For the normal CMOS technology, the smallest component mismatch that can be achieved is on the order of $0.1\% - 0.5\%$. So the non-linearity of the multi-bit internal DAC can not be neglected.

To study the effect of the non-linearity from DAC on the modulator system, the non-linearity in the modulator is modelled as additive noise sources, as shown in Figure 42. In Figure 42, $v1$ represents the errors before the quantizer such as non-linearity generated by the filter H or by the gain blocks of the controller. $v2$ represents the errors of the internal DAC. Similar with the sigma-delta modulator, all the errors before the quantizer would be suppressed by the modulator [6]. However, the non-linearity of the internal DAC is fed to the system input directly. Thus the errors can not be reduced by the negative feedback [4].

So the ultimate linearity of the modulator is no better than the linearity of the multi-bit internal DAC.

In this project a 14-bit resolution is needed. Low-cost CMOS technologies usually offer 10-bit matching accuracy. Several approaches can be used to improve the linearity performance of the DAC. One approach is to use dynamic element matching (DEM) to randomize the nonlinearity caused by mismatch. Another approach is to calibrate each unit current source by using a master reference. We choose the latter one, current calibration, to improve the matching accuracy of the current sources.

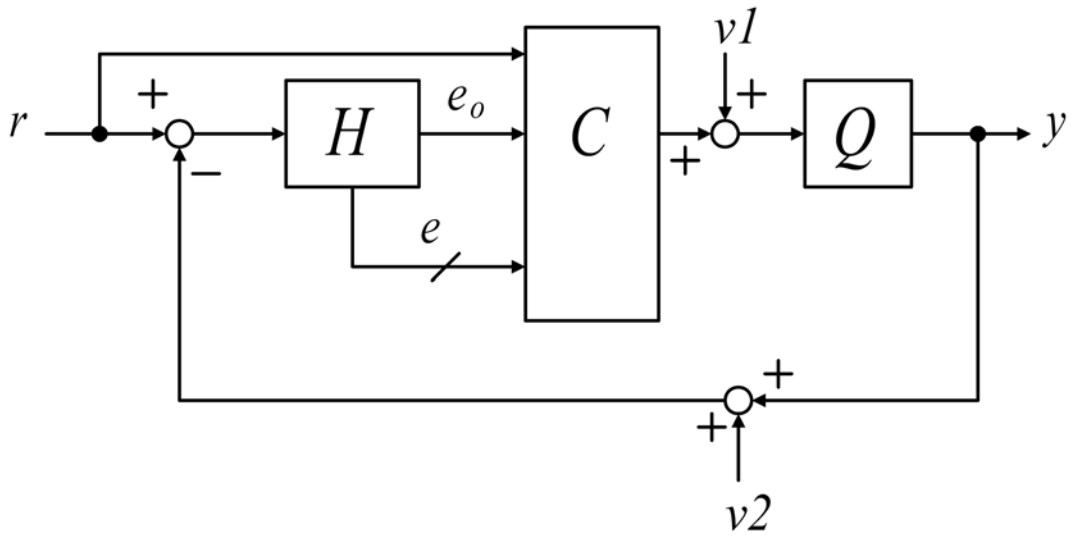

Fig. 42. Block diagram of the modulator with non-linearity effect from feedback DAC

The current calibration principle is illustrated in Figure 43 [28]. This technique makes each unit current source equal to the reference current I_{REF}, thus canceling errors due to mismatch.

During calibration mode, $S1$ and $S2$ are closed. The current difference between the reference current I_{REF} and the drain current of $M1$, $I1$, is forced to flow through $M2$, thus generating a voltage drop V_{GS} on $M2$. $I_{REF} = I1 + I2$. In work mode, $S1$ and $S2$ are opened. As V_{GS} of $M2$ is stored on C_H, the drain current of $M2$ remains the same $I2$. Thus the total output of the unit current source keeps as I_{REF}.

The key point in this circuit is to control $I1$ as 99% of the total current, I_{REF} because when $I2$ is quite small, $M2$ can be a long device to attain better matching and lower sensitivity to charge injection at its gate.

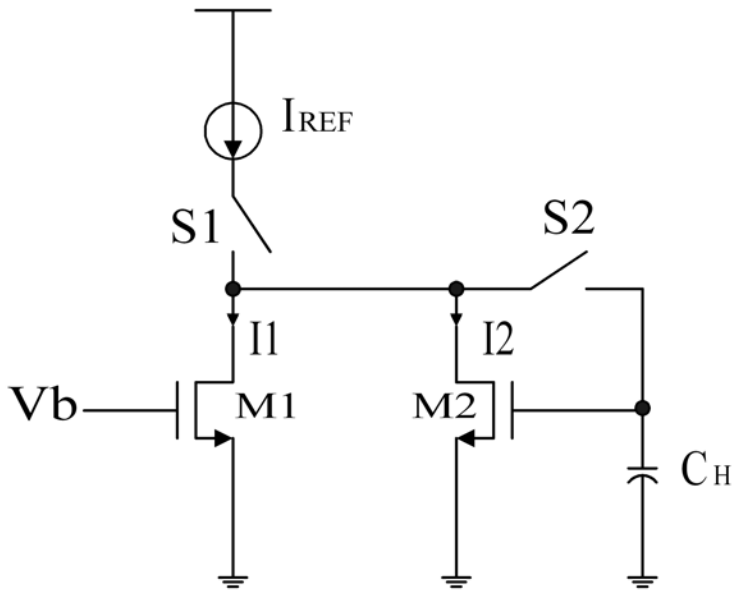

Fig. 43. Principle topology of the current calibration circuit

The circuit of Figure 43 has two drawbacks. First, it requires a large C_H to suppress the effect of feed-through due to $S2$ because the adjustable current source has single-ended control. Second, if $I1 > I_{REF}$, calibration circuit fails to operate. But it's difficult to ensure that $I1$ is less than I_{REF} by only 1%.

Figure 44 shows a differential bi-directional current calibration circuit which can overcomes the above drawbacks [28].

The OTA formed by $M5$, $M6$, $M7$ and $M8$ can source and sink output current. The differential structure can overcome the feed-through errors.

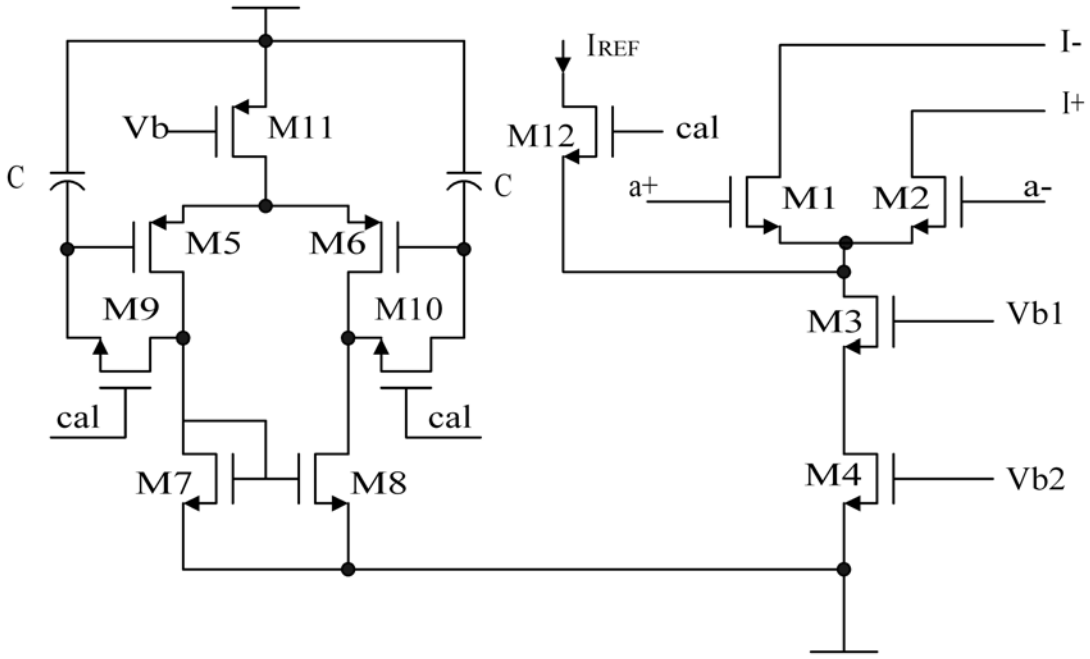

Fig. 44. Schematic of the differential bidirectional current calibration circuit

3. Calibration Control Circuit

When the circuit is initialized by switching the power on, the chip will calibrate the 16 unit current sources first. To control the operation of calibration, we design a calibration control circuit. My friend Nebu John Mathai helped me in this digital block design.

The output sequence of calibration control circuit is shown in Figure 45. In the first clock cycle, all control output are low except $A1$ is high, which calibrates the first unit current source by closing the switches $S1$ and $S2$ in this current source (see Figure 43). In the second clock circle, $A2$ is high $\cdots$. The unit current sources would be calibrated one by one in this way.

Figure 46 shows the topology of the calibration control circuit. It consists of

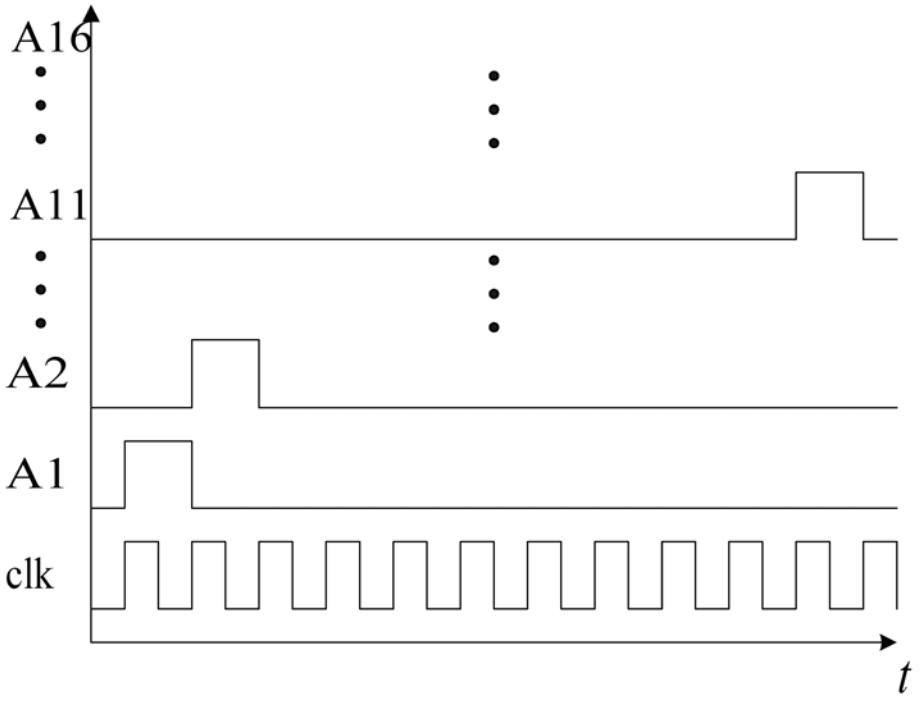

Fig. 45. Output sequence of calibration control circuit

four D-latches, one adder and one binary-to-thermometer decoder [35] [36] [37]. The output of the decoder is the output signal to control the calibration sequence.

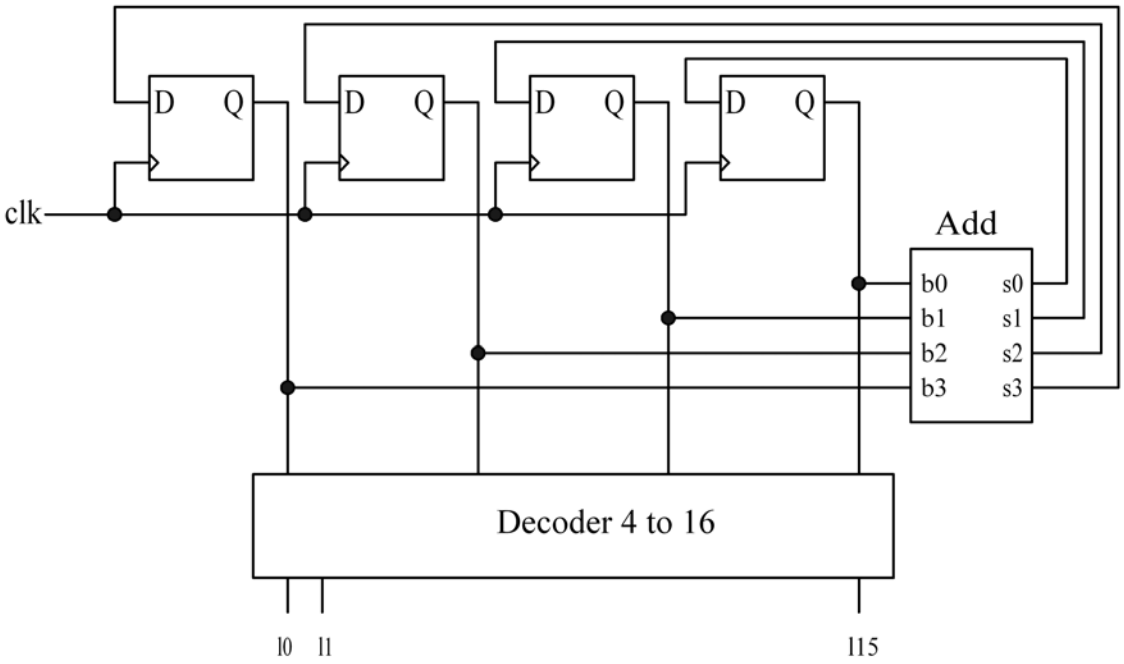

Fig. 46. Topology of the calibration control circuit

The schematic of the adder block is shown in Figure 47.

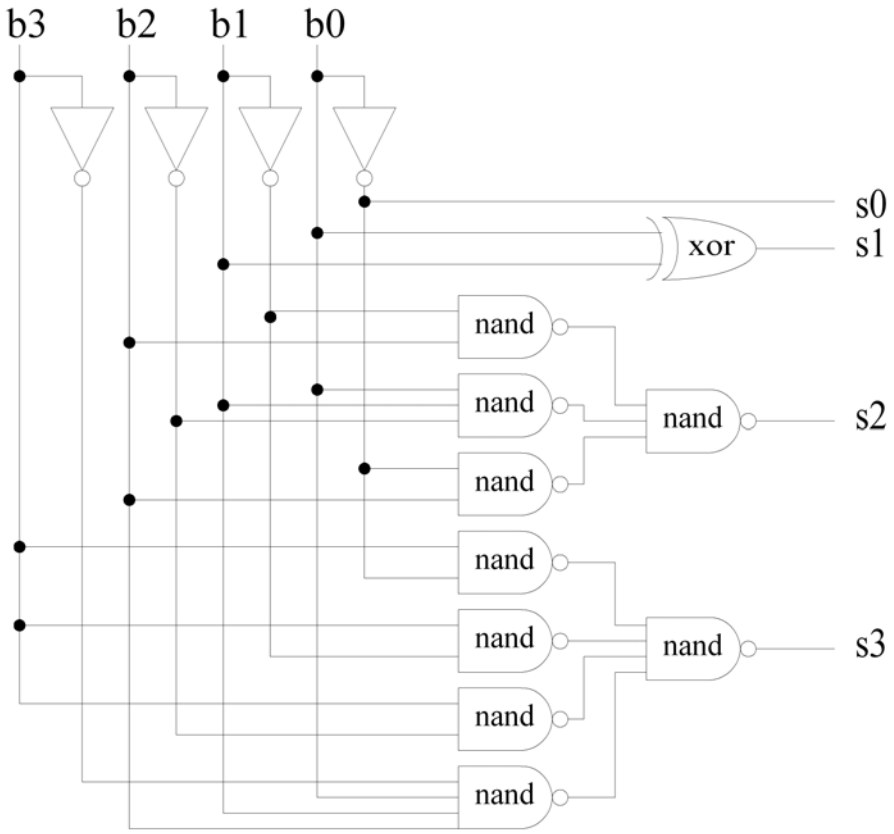

Fig. 47. Schematic of the adder block

The illustration topology of the binary-to-thermometer decoder is shown in Figure 48. The input signals are $s0$, $s1$, $s2$ and $s3$. The output signals are $A1$, $A2$, $\cdots$, $A16$. The logic between input and output is:

A1=Nor(s3, s2, s1, s0)

A2=Nor(s3, s2, s1, ns0)

A3=Nor(s3, s2, ns1, s0)

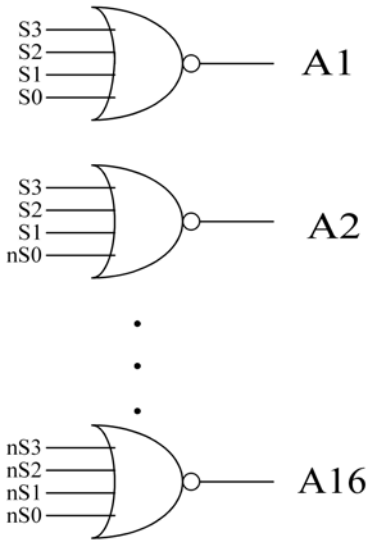

Fig. 48. Illustration topology of the binary-to-thermometer decoder

A4=Nor(s3, s2, ns1, ns0)

A5=Nor(s3, ns2, s1, s0)

A6=Nor(s3, ns2, s1, ns0)

A7=Nor(s3, ns2, ns1, s0)

A8=Nor(s3, ns2, ns1, ns0)

A9=Nor(ns3, s2, s1, s0)

A10=Nor(ns3, s2, s1, ns0)

A11=Nor(ns3, s2, ns1, s0)

A12=Nor(ns3, s2, ns1, ns0)

A13=Nor(ns3, ns2, s1, s0)

A14=Nor(ns3, ns2, s1, ns0)

A15=Nor(ns3, ns2, ns1, s0)

A16=Nor(ns3, ns2, ns1, ns0)

Here

ns0=Not(s0)

ns1=Not(s1)

ns2=Not(s2)

ns3=Not(s3)

To reduce the propagation delay of the digital circuit, we design the size of the transistors carefully. When sizing the transistors in a gate with multiple fan-in's, we should pick the combination of inputs that triggers the worst-case conditions [35] [36] [37].

For example, for a NAND gate, which is shown in Figure 49, to have the same pull-down delay as a minimum sized inverter (i.e., NMOS: 0.6μm/0.4μm and PMOS: 1.8μm/0.4μm), the NMOS devices in the NAND stack must be made twice as large (i.e., NMOS of NAND should be 1.2μm/0.4μm) so that the equivalent resistance the NAND pull-down is the same as the inverter. The PMOS device can remain unchanged.

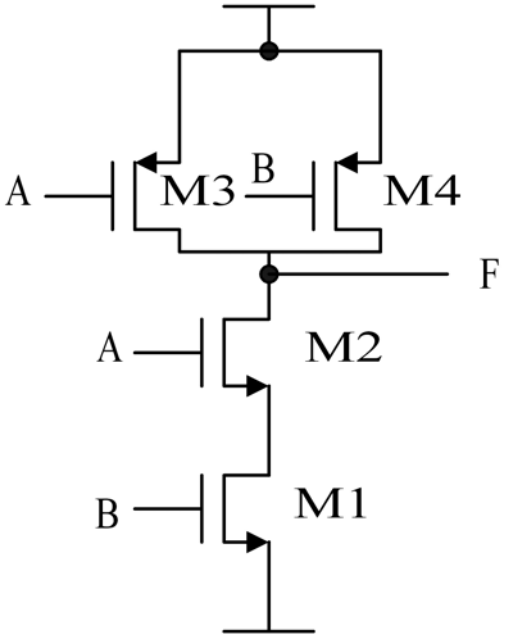

Fig. 49. Schematic of a NAND gate

CHAPTER VI

LAYOUT DESIGN AND POST-LAYOUT SIMULATION RESULTS

A prototype circuit of the novel oversampling modulator proposed in previous chapters is implemented in a 0.35-μm double-poly CMOS technology process (TSMC35_P2) through MOSIS. Figure 50 shows the layout of the chip. The dimensions of the design are $2150 \times 2150\mu\text{m}^2$ without pads and $2850 \times 2850\mu\text{m}^2$ with pads.

For a high-quality layout, there are mainly two important issues that should be considered: matching and noise issues [38] [39]. For good matching, symmetric structures are adopted for most of the cells, including transistors, resistors and capacitors. Dummy cells are also used in the sensitive parts to eliminate the boundary effects. To reduce coupling of noise, such layout technologies are adopted:

- The sensitive analog blocks and noisy digital blocks are separated in terms of physical positioning. As shown in Figure 50, the most sensitive analog blocks, such as the filter and the controller, are placed far away from digital blocks, such as the clock generation circuits and the current calibration control circuits.

- Separate analog and digital power supplies are used to reduce the interference from digital circuits to analog circuits due to the large glitch injected on the digital supply when the digital gates change states.

- The analog and digital circuits are separated by guard rings and wells connected to the power-supply voltages to reduce substrate coupling. For the mixed signal blocks, flash ADC and DAC, the analog cells are also separated by guard rings and wells from digital cells.

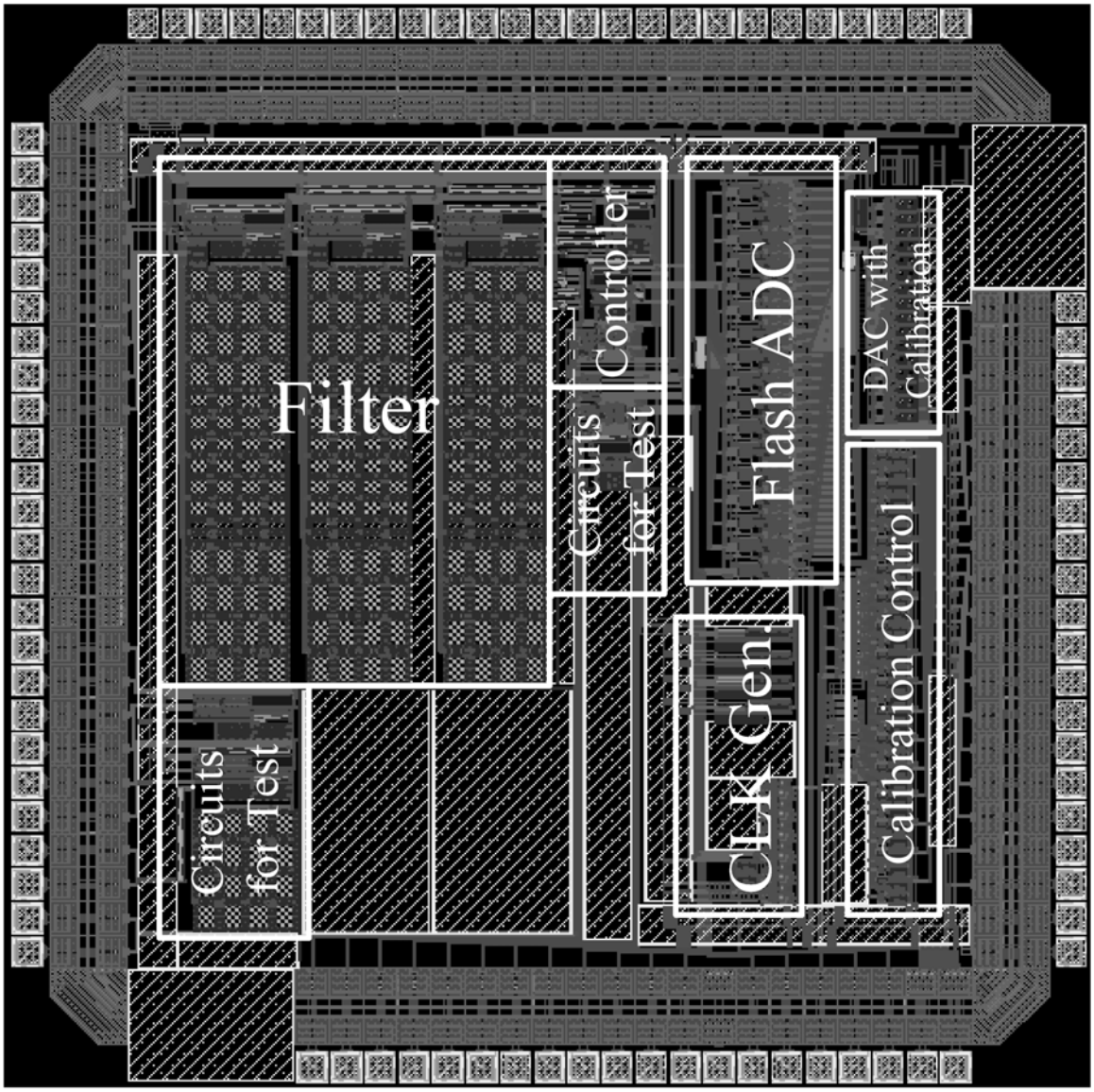

Fig. 50. Layout of the prototype oversamping modulator

- Enough ties to the power supplies are placed near the transistors to minimize voltage drops.
- Unused areas are filled with capacitors for decoupling power supplies.
- Crossing routing is used to avoid parasitic capacitances.

The diagram of the on-chip voltage buffer is shown in Figure 51.

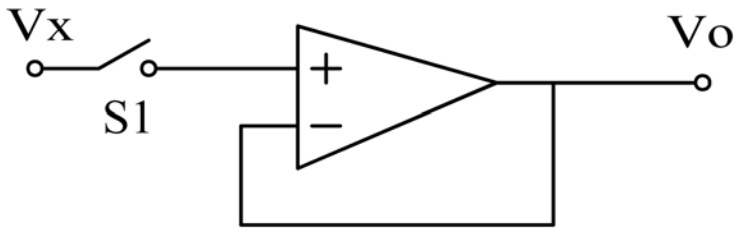

Fig. 51. Diagram of the on-chip voltage buffer

To inspect the node voltage, the switch in the buffer is closed. The voltage is led off-chip by the unity gain buffer. To minimize the effect of the buffer, the switch is kept open in normal simulations.

Because the accuracy requirement for the buffer is not very high, the opamp in this buffer is designed as a simple one-stage amplifier.

Because the post-layout simulation is especially time-consuming, we only did 5 simulations for different input amplitudes. The dynamic range plot of the modulator is shown in Figure 52.

The performance of the prototype oversampling modulator obtained by post-layout simulation is summarized as shown in Table XIII.

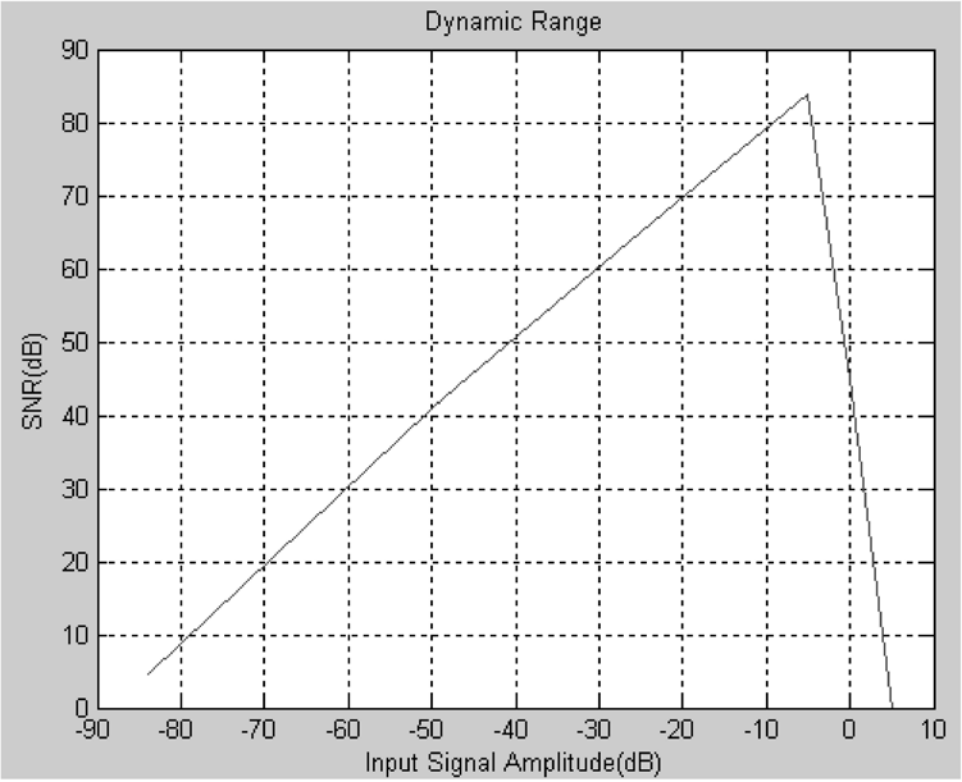

Fig. 52. Dynamic range of the prototype oversampling modulator in post-layout simulation

Testing results are currently in progress and we aim for completion before May 2005.

Table XIV shows the performance of two most recent continous-time sigma-delta publications [9] [40].

The data show that the performance of our work is close to the performance of the recent sigma-delta modulators, even though this is the first circuit implementation of the NCO modulator, while the sigma-delta modulation already developed for fifty

Table XIII. Performance of the prototype oversampling modulator obtained by post-layout simulation

Signal Bandwidth	500KHz
Sampling Frequency	32MHz
OSR	32
Peak SQNR	83.7dB
Dynamic Range	90dB
Supply Voltage	$\pm$1.65V
Power Consumption	60mW
Area	$2150 \times 2150 \mu m^2$
Process	0.35-μm CMOS (TSMC35_P2)

Table XIV. Performance of two most recent continous-time sigma-delta publications

	[9](Jan. 2004)	[40] (Nov. 2004)
Signal Bandwidth	1.1MHz	1.23MHz
Sampling Frequency	35.2MHz	2GHz
OSR	16	813
Peak SNR	84dB	79dB
Supply Voltage	3.3V	1.8V
Power Consumption	62mW	18mW
Area	$2.4 \times 2.4 mm^2$	0.89 mm^2
Process	0.5-μm CMOS	0.18-μm CMOS

years. This prototype NCO modulator circuit is designed very conservatively. Higher performance, such as higher SQNR, wider signal bandwidth or less power, can be achieved by optimizing the design of the modulator.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

A. Conclusions

This work is the first circuit implementation of the NCO modulator proposed by Dr. Takis Zourntos. It shows that this novel oversampling modulation theory can be cost-effectively realized into circuits with good performance. This is an exciting result because this novel oversampling modulation theory is theoretically stable. With a reduced stability constraint, the NCO modulator may potentially achieve higher SNR or less power by designing the modulator more aggressively.

The simulation results show that 90dB dynamic range over a 500kHz input signal bandwidth is achieved by this third-order continuous-time oversampling modulator with 4-bit internal quantization realized in a 0.35-μm double-poly CMOS technology process.

The principal contributions of this work are:

1. The characteristics of the NCO modulator is further explored, especially the effect of the non-idealities, errors on voltage reference and feedback loop delay.

2. A new filter circuit is proposed to realize the filter with the special requirements: a series of filter state outputs for the controller, realizing arbitrary zeros and poles, high linearity and robustness to process variation.

3. Two types of comparators with synchronization latches to eliminate the effect of metastability are proposed for the sgn() block and internal flash ADC.

4. A new DAC with current calibration circuits for high linearity is proposed.

5. A deliberate clock scheme is used to overwhelm the effect of the non-ideal time delay of comparators.

6. Most importantly, the first prototype circuit of the novel oversampling modulator is implemented. Simulation results show it achieves 83.7-dB peak SQNR, 90-dB dynamic range over a 500kHz input signal bandwidth, and 60 mW power consumption. These results are quite good because most of the blocks are designed very conservatively. Higher performance, such as higher SQNR, higher signal bandwidth or less power, can be achieved by optimizing the design of the modulator.

B. Suggestions for Future Work

This is the first step to implement the NCO modulator. There are a lot of choices to further develop this new class of oversampling modulators. Below are some of the possibilities:

- Optimize the design of the modulator for higher performance. Also the different OSR, order and internal quantizer resolution can be investigated for different performance requirement. It is possible that some unexplored advantages exist.

- Develop the new oversampling modulation theory for discrete-time applications. Then the switched-capacitor techniques can be used to implement the modulator. The majority of the sigma-delta modulators employ switched-capacitor loop integrators. That would be a good choice for developing this NCO modulator.

- Develop this novel oversampling modulation scheme for other applications such as digital-to-analog conversion, PLL, Class-D power amplifiers, and other signal

processing devices in which sigma-delta modulators are used.

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